DATA SHEET

D9020ASIA

Advanced Signal Integrity Software for Infiniium Oscilloscopes

D9020ASIA is intended for any customer working in high speed digital applications where eyes are closed. Equalization, InfiniiSim, and Crosstalk/Power Integrity packages enable deep analysis as to why an eye is closed, and what it will take to open it. It is available on all Infiniium oscilloscopes.

KEYSIGHT TECHNOLOGIES

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Background: Why Equalize?

As data rates go up, the signal deteriorates from the transmitter to the receiver due to ISI, noise, and other factors. The more loss that occurs, the more difficult it is for a receiver comparator to distinguish a “1” from a “0”. A high data rate coupled with a lossy channel will cause an open eye at a transmitter to be closed at the receiver. Receivers need to be able to evaluate 1s and 0s. As eyes get more and more closed, the receiver has a more difficult time interpreting the correct value as a 1 or a 0. This difficulty ultimately leads to significant data corruption and errors. Equalization uses advanced filtering techniques to correct the voltage level of the current bit. By removing much of the intersymbol interference through filtering, equalization can improve closed eyes into open eyes and significantly reduce the data corruption. The equalization software provides insight into designers’ equalizer designs and key data into the viability of the channel link after equalization.

It is also important to use an oscilloscope with low noise. If an oscilloscope has the lowest noise, the equalization technique will open the eye wider. Keep in mind that equalization will amplify any noise not caused by ISI, which includes oscilloscope noise. Infiniium oscilloscopes have the industry’s lowest noise floor, so there is much less noise to be amplified. This results in greater equalization accuracy.

Equalization requires the oscilloscope to know where the clock transitions. Clock data recovery allows the scope to know where the transition occurs, making equalization possible. Full clock data recovery can only be found in the serial data analysis software package, which is standard on any Infiniium oscilloscope with software 6.30 or greater.

Product Overview

The Keysight Technologies, Inc. serial data equalization (SDE) software for Infiniium Series oscilloscopes provides fast and accurate equalization simulating decision feedback equalization (DFE), feed-forward equalization (FFE), and continuous time linear equalization (CTLE) modeling in real time. SDE software allows users to input their own self-designated tap values or it will find the optimal tap values for the designer for FFE and DFE. CTLE allows DC gain and up to three-pole modeling.

Used in conjunction with the Infiniium Series scopes’ unique Infiniium data accelerator (IDA) chip, SDE software provides fast update rates and rapid analysis of real-time eyes that have been partially or fully closed by the serial data link. The SDE software package includes a wizard that provides an easy-to-follow, step-by-step process to set up and emulate full equalization. D9020ASIA is compatible with all Infiniium oscilloscopes with software 6.30 or higher.

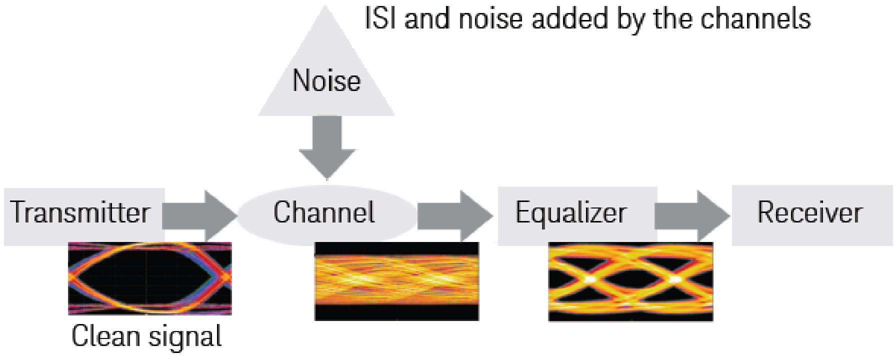


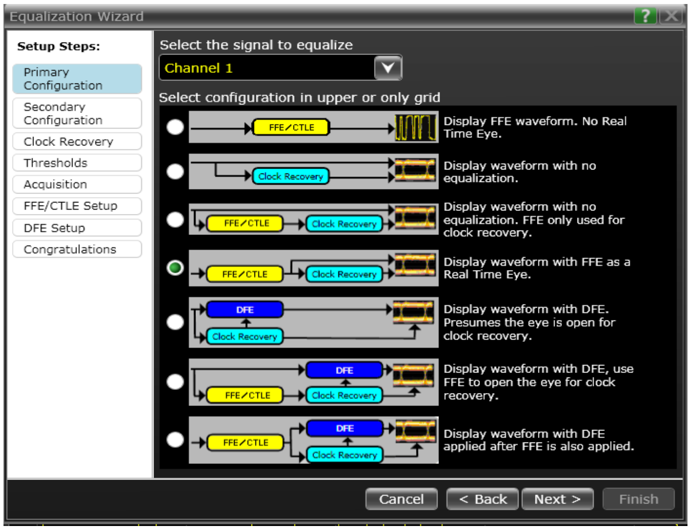
Figure 1. A complete link.

Serial Data Equalization

Easy equalization setup

The serial data equalization software extends the ease-of-use advantages of Keysight's Infiniium oscilloscopes to complete analysis of the receiver. The equalization wizard walks you quickly through the steps required to setup and perform equalization. Intuitive displays and clear labeling of information make it easy to perform complex equalization emulation. The SDE wizard walks you through seven different equalization scenarios.

1. FFE or CTLE are emulated, but the real time eye is not displayed. You will see only the waveform. This option lets you use the equalized waveform to perform further analysis on it such as jitter decompensation.



Select the signal to equalize: Channel 1

Select configuration in upper or only grid

○ Display FFE waveform. No Real Time Eye.

○ Display waveform with no equalization.

○ Display waveform with no equalization. FFE only used for clock recovery.

● Display waveform with FFE as a Real Time Eye.

○ Display waveform with DFE. Presumes the eye is open for clock recovery.

○ Display waveform with DFE, use FFE to open the eye for clock recovery.

○ Display waveform with DFE applied after FFE is also applied.

Figure 2. Equalization options in the wizard.

2. No equalization applied. Option 2 is to see the eye with no equalization applied. The option works great for comparing the impact of different equalization techniques.

3. FFE or CTLE are applied only to recover the clock, and the referenced eye is un-equalized. As real time eyes get closer to being fully closed, it can be difficult for the software to recover a clock because it can be difficult to distinguish between a 1 and 0 and provide the correct data rate. This option makes it possible to easily recover the clock, even on closed eyes.

4. FFE or CTLE emulation.

5. Standard DFE emulation. One caveat for this option is that if your real time eye is closed, the DFE will not work correctly. You will need to use the next option to use FFE or CTLE to open the eye a little bit and then use DFE.

6. Standard DFE emulation for a closed eye. Note that FFE or CTLE is used to recover the clock but is not displayed in the real time eye.

7. FFE and then DFE is applied to the real time eye. Both are displayed in the resulting real time eye.

CTLE, FFE and DFE Emulation

The SDE software provides full emulation of decision feedback, feed-forward, and continuous time linear equalization. The software provides the flexibility to compare real time eyes of a non-equalized waveform versus an equalized waveform, or to compare a DFE waveform versus an FFE or CTLE waveform.

SDE software allows you to quickly compare different tap values. Tap values are dimensionless correction factors applied to the bit voltage levels in serial data patterns during equalization. Tap values can be viewed as the ratio of the voltage the receiver should have seen versus what the receiver actually saw. Accurate tap values are essential for modeling an ideal real time eye at the receiver. Serial data equalization software will save you time by modeling up to forty tap values for you. In addition to this, you can use the serial data equalization software package to find what combination of tap values will maximize eye height. SDE software provides precursor tap functionality for FFE emulation.

Serial data equalization provides multiple inputs including an “eye width” option that optimizes the tap values based on whether the designer wants a wider or higher eye. Unlike some equalization emulation packages, serial data equalization works on any pattern and the software does not need to know the pattern the designer is using.

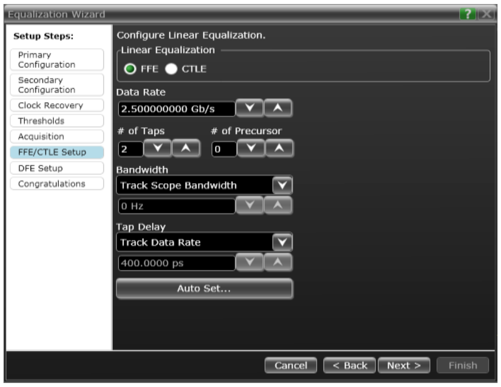
Continuous Time Linear Equalization (CTLE)

Many of today’s standards require CTLE as part of compliance testing. SDE software makes verifying emulation easy. Simply enter your DC gain value, zero frequency, and pole1 and pole2 frequency values to verify your design. Serial data equalization also supports USB 3.1’s specific CTLE.

Flexible clock recovery

Choose constant-frequency, first-order phase-locked loop (PLL), second-order PLL clock recovery, explicit clock, explicit first order PLL, explicit second order PLL or FibreChannel clock recovery methods. Adjust the center frequency and bandwidth, and in the case of second-order PLL, the damping factor.

New to the equalization software is the equalized first and second order PLL, which allows you to recover the clock on a closed eye. This is accomplished by first applying FFE or CTLE to the waveform and then recovering the clock, making clock recovery possible even on closed eyes.



Equalization Wizard

Setup Steps:
- Primary Configuration
- Secondary Configuration
- Clock Recovery
- Thresholds
- Acquisition
- FFE/CTLE Setup
- DFE Setup
- Congratulations

Configure Linear Equalization.

Linear Equalization: ● FFE ○ CTLE

Data Rate: 2.500000000 Gb/s

# of Taps: 2

# of Precursor: 0

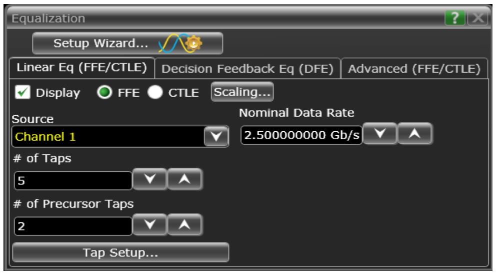
Bandwidth: Track Scope Bandwidth

0 Hz

Tap Delay: Track Data Rate

400.0000 ps

Figure 3. Linear equalization setup in the wizard.



Equalization

☑ Display ● FFE ○ CTLE

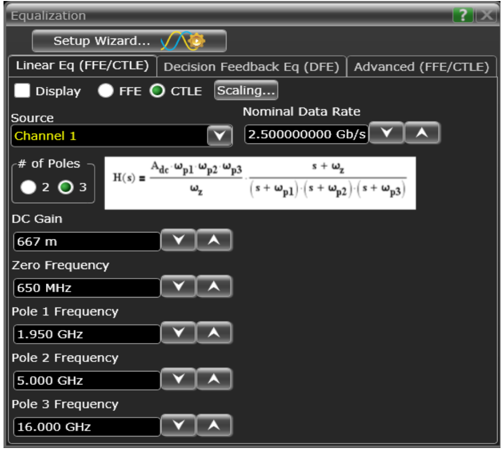
Source: Channel 1

Nominal Data Rate: 2.500000000 Gb/s

# of Taps: 5

# of Precursor Taps: 2

Figure 4. The wizard allows you to choose FFE, CTLE, or DFE.



Equalization

□ Display ○ FFE ● CTLE

Source: Channel 1

Nominal Data Rate: 2.500000000 Gb/s

# of Poles: ○ 2 ● 3

$$H(s) = \frac{A_{dc} \cdot \omega_{p1} \cdot \omega_{p2} \cdot \omega_{p3}}{\omega_z} \cdot \frac{s + \omega_z}{(s + \omega_{p1}) \cdot (s + \omega_{p2}) \cdot (s + \omega_{p3})}$$

DC Gain: 667 m

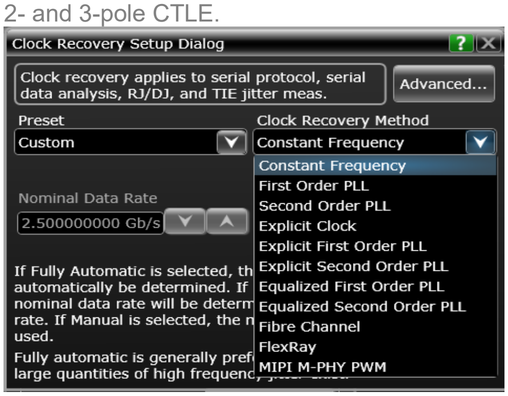
Zero Frequency: 650 MHz

Pole 1 Frequency: 1.950 GHz

Pole 2 Frequency: 5.000 GHz

Pole 3 Frequency: 16.000 GHz

Figure 5. Serial data equalization supports both 2- and 3-pole CTLE.



Clock Recovery Setup Dialog

Clock recovery applies to serial protocol, serial data analysis, RJ/DJ, and TIE jitter meas.

Preset: Custom

Clock Recovery Method: Constant Frequency

Nominal Data Rate: 2.500000000 Gb/s

If Fully Automatic is selected, th
automatically be determined. If
nominal data rate will be determ
rate. If Manual is selected, the n
used.

Fully automatic is generally pref
large quantities of high frequenc

Figure 6. Clock recovery set up.

Crosstalk Analysis

Why is this important?

Increased data communication speeds and circuit density of mobile devices has led to very high serial data rates on multiple lanes, placed very close together. This combination leads to an increased amount of crosstalk distortion between serial data signals. As a result, crosstalk is becoming a more important problem to diagnose and quantify. Integrated circuit power supplies are also increasingly susceptible to crosstalk at these higher serial data rates. Simultaneous switching noise (SSN) and ground bounce from serial data signals and switching power supplies can create perturbations on the supplies that distort the data lanes they drive in the form of noise and jitter.

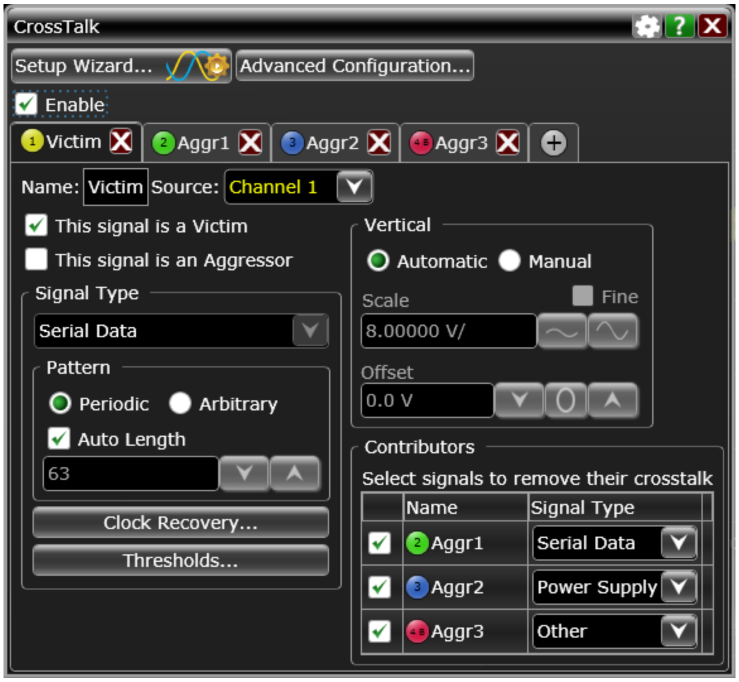
The need to troubleshoot and characterize crosstalk is not new, but the legacy methods of measuring crosstalk in digital communications systems has relied on the process of selectively disabling some channels while enabling others. This requires measuring the crosstalk effects in the system while operating in special test modes, which means measuring them under abnormal conditions. Worse yet, some systems cannot even operate the necessary special modes.

Our solution

Keysight has developed a crosstalk analysis application to assist in the diagnosis and quantification of crosstalk that does not require the system under test to operate in any special test modes. The application works by constructing optimal models of the crosstalk mechanisms between multiple measured signals. The user, for example, can acquire up four signals simultaneously of a running system and then configure the application to calculate the optimal crosstalk models between them. Once these models are known, various victim signals can be displayed with and without the crosstalk from each aggressor. In this way, noise, jitter and eye-diagram measurements can be made on the victim with and without crosstalk to quantify the amount each aggressor contributes to each of these measurement values.

The application not only detects and quantifies the presence of crosstalk, but it can also determine the relative magnitude of error each aggressor imparts to the victim. It can also go one step further by actually removing the crosstalk from the victim so you can visually compare the original waveform with the clean waveform side-by-side. You can compare the “before” and “after” waveforms directly on the scope display or by comparing the results from other scope analysis tools such as real-time eye diagrams or jitter analysis. This approach gives you a direct way of quantifying the amount of improvement you can expect by mitigating the different sources of crosstalk.

The crosstalk analysis application can provide a lot of valuable insight into your design. For instance, it can help you determine the margins the design would recover without the crosstalk. It can also help determine if a signal failing design specification would pass without the crosstalk. This approach can lead to important design decisions on whether it is worth the time and effort to improve the crosstalk effect and where in the board to make improvements.



☑ Enable

Name: Victim Source: Channel 1

☑ This signal is a Victim
□ This signal is an Aggressor

Signal Type: Serial Data

Pattern: ● Periodic ○ Arbitrary
☑ Auto Length: 63

Vertical: ● Automatic ○ Manual
Scale: 8.00000 V/ □ Fine
Offset: 0.0 V

Contributors
Select signals to remove their crosstalk

	Name	Signal Type
☑	Aggr1	Serial Data
☑	Aggr2	Power Supply
☑	Aggr3	Other

Figure 7. Keysight crosstalk analysis application for analyzing serial data, power supply and other sources of crosstalk effect to the victim signal. Up to four signals can be analyzed at once.

Features of the crosstalk analysis application include:

- Analysis of up to four signals (aggressors or victims) at once.
- No crosstalk simulation or model is required when performing crosstalk analysis.
- Identify and report the amount of crosstalk present on victims from each aggressor.
- Plot waveforms without crosstalk. Compare them with the original waveforms using scope tools such as eye diagram and jitter separation to see how much margin can be recovered.
- Setup wizard to guide user through setting up the aggressors and victims and running the crosstalk analysis.

Types of crosstalk

Transmission line crosstalk

Parallel transmission lines are prime candidates for crosstalk. The mutual inductance and capacitance between them allows energy to couple from one lane into another. The voltage generated by capacitive coupling creates a current that travels in both directions, whereas the inductive coupling creates a current that travels only in the reverse direction. When added together, the two currents reinforce each other in the reverse direction but cancel each other out (at least to some extent) in the forward direction. The reverse traveling wave returns back to the transmitter end and is called “near-end” crosstalk (NEXT), while the forward traveling wave arrives at the receiver end and is called “far-end” crosstalk (FEXT). The magnitude and shape of these waveforms are quite different from each other.

Power supply aggressor crosstalk

Power supplies can also be a significant source of interference on a data line, creating both noise and jitter. This type of interference may simply be referred to as “power supply noise,” but its effects are similar to traditional crosstalk, and so it is straightforward to think of a power supply as just another source of crosstalk.

Noise and voltage drift in a power supply can affect the timing of the serial data waveforms they are driving. Timing errors can occur through a number of different mechanisms, such as phase changes which are caused by voltage-dependent driver impedances and frequency changes caused by voltage-controlled oscillators. The resulting jitter is called power supply induced jitter (PSIJ).

In another case, the power supply may be directly connected to the transmission line when the logic level switches to that value. Noise and bias on the voltage rail can therefore transfer directly to the bit stream. While this seems straightforward, it is more complicated than the parallel transmission line case. The interference may be present only when the bit stream is at a particular logic level (for Vcc aggressors it might present only when the logic level is high, whereas for GND aggressors it might present only when the logic level is low). It is therefore possible to have the high voltage bits experience a lot of noise while the low bits have little (or vice versa). This is a non-linear (or voltage-dependent) type of interference.

Power supply victim crosstalk

The signal integrity of power supply voltages (including ground) can be affected by the circuits they are driving. One common example of this is simultaneous switching noise (SSN), which can produce ground bounce (the Vcc rail can also “bounce” and may be referred to as Vcc sag). SSN can occur as a result of parasitic inductances that lie between the device (chip) ground and the system (board) ground.

As the voltage on the output changes state, it draws a current through the switching transistors. As that current flows to ground, it causes a voltage drop across the parasitic inductances. That voltage drop in turn changes the voltage you would measure at the device ground. The voltage measured there may bounce up and down in correlation with data transitions. The effect is amplified when more than one line is switching states at the same time since this will draw more current. In addition, depending on the impedance and the various switching delays, the ground bounce may appear to have a ringing effect as well.

Crosstalk network models

The crosstalk application constructs different types of crosstalk models from the measured waveforms depending on the victim and aggressor signal types. In the simplest case, when both victim and aggressor are serial data signals, the model is a linear n-port transfer function model. Figure 2 is simple example of a 2-channel serial data system. Physically, the transmission system consists of two transmitters, two receivers and a 4-port linear network model connected between them. Probing the two serial data channels provides the input waveforms to the crosstalk application.

The application begins analyzing the waveforms by extracting the serial clock and data pattern of each. It then uses the ideal data pattern as input to the 4-port linear crosstalk model shown in figure 3. It computes the best-fit transfer function model, which transforms the ideal waveforms into the actual measured waveforms. Within the model, h11 and h22 represent the signal's ISI while h21 and h12 represent the coupling or crosstalk between the two signals. This approach allows the crosstalk analysis application to remove the effect of either the crosstalk, ISI or both crosstalk and ISI from the measured waveforms.

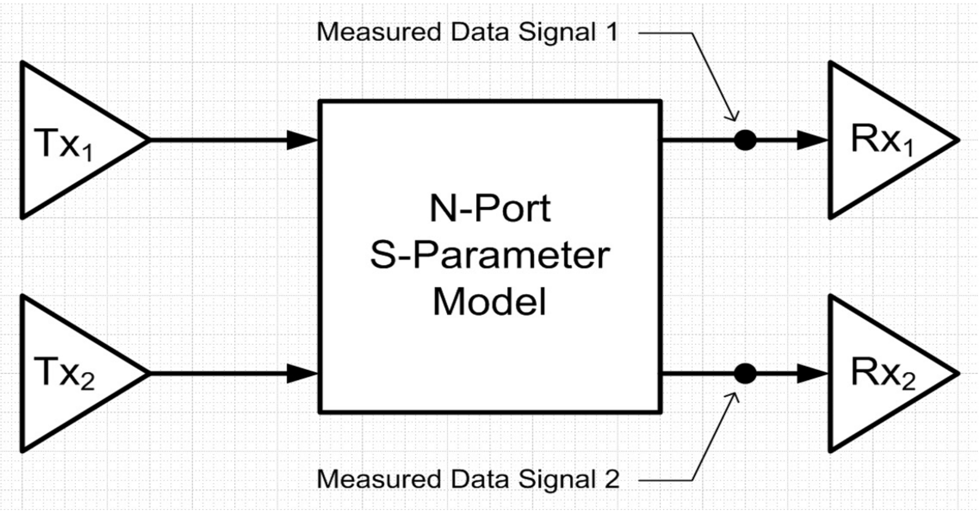


Figure 8. A 4-port network model for two parallel transmission lines. The black dots show possible probe locations at the far end.

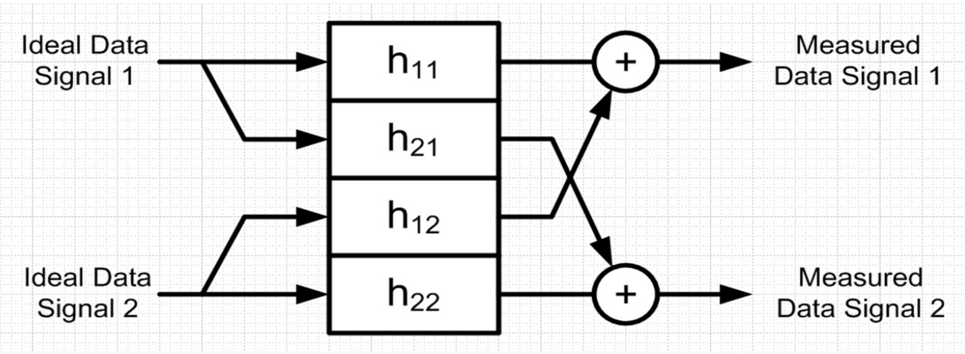


Figure 9. The crosstalk analysis application computes a 4-port linear crosstalk model, which transforms the ideal waveforms into the actual measured waveforms.

Crosstalk analysis challenges solved

One way to uncover the network model behavior and estimate its parameters is to selectively turn off the victim and/or aggressor waveforms. For example, you could visualize the crosstalk that channel 1 receives by turning off channel 1 and turning on channel 2. The resulting waveform on channel 1 would be pure crosstalk (and noise). Alternatively, you could do the reverse by turning on channel 1 and turning off channel 2. The resulting waveform on channel 2 would represent a clean output without any crosstalk from channel 1. To quantify the relationships, you could do measurements on the different waveforms, such as peak-to-peak voltage measurements or eye diagrams.

While straightforward, there are a number of problems with this approach. First, it may not be possible or convenient to selectively enable or disable the different data streams. Second, the approach is tedious and time consuming. In a 4-lane system, for example, there are 16 victim-aggressor pairs (if you include ISI), which leads to a large number of test setups, measurements and results that are seen separately and must be manually recorded. Third, because the measurements are not simultaneous, any constructive or deconstructive interference effects will be lost. Fourth, the approach simply would not work if the source of interference comes from outside the network, such as from a power-supply that cannot be disabled.

The Keysight crosstalk tool solves these problems by estimating the network model from a single test setup using a simultaneous acquisition of all data lanes. The model can be constructed by simply probing each transmission line using the oscilloscope and then enabling the application. After constructing the model, the application will display some measurement results, such as the magnitude of the crosstalk for each victim-aggressor pair and will also display a crosstalk-removed or “clean” waveform. The crosstalk-removed waveform simulates what the waveform would look like if the specified aggressors were disabled. The waveform is treated like any other waveform on the scope and can therefore be used as an input to any other oscilloscope measurement or analysis. You can easily see, for example, the before and after eye diagrams or compare the before and after jitter components using D9010JITA/D9020JITA.

Test setup

Probing

To create a test setup for crosstalk, simply probe all of the transmission lanes and power supplies that are to be included in the analysis. The application currently supports a total of four input waveforms.

For serial data signals, it is best to probe all the victim lanes at the receiver end. This captures the actual waveforms that are delivered to the receiver. For perfectly-terminated transmission lines, this probing scheme will capture primarily FEXT since NEXT travels back toward the receiver end. However, it’s possible for a received waveform to contain elements of both FEXT and NEXT. To specifically analyze NEXT, one can probe at the transmitter end. In the crosstalk tool you do not need to specify a NEXT or FEXT measurement; The application will measure the crosstalk that is present regardless of what type it is.

For power supply aggressor crosstalk, it is also best to probe the victim lanes at the receiver end. The power supply aggressor can be probed anywhere. Keep in mind that supplies of both the transmitter and receiver can contribute to crosstalk.

For power supply victim crosstalk, it does not matter where you probe the victim or the aggressors in this case. It is possible to have up to three aggressors, but all of them must be serial data aggressors. This requirement is because ground bounce is a result of the current drawn from a supply during data transitions, so it is necessary to find those transitions. Only one power supply victim can be analyzed at a time due to the complexity of the algorithm.

Synchronization

Another consideration in the test setup is synchronization. Because the application is looking for correlations between victims and aggressors, all victims and aggressors need to be acquired simultaneously. That application accommodates time skews between victims and aggressors. However, minimizing this skew can improve calculation time measurement results.

Test patterns

The crosstalk application will work with arbitrary serial data patterns, though periodic patterns produce better results with a shorter calculation time. Note also that in order to distinguish between distortions cause by ISI and the various aggressors, each serial data channel must transmit different patterns or run at different data rates. Note that longer data patterns are not necessarily helpful or desirable in the crosstalk analysis tool. One reason is simply practicality. A jitter analysis tool looks only at timing errors in the data, so it only needs to process one data point per data edge (transition), whereas the crosstalk tool uses all of the waveform data. Therefore, moderate lengths up to 211 - 1 or less are recommended.

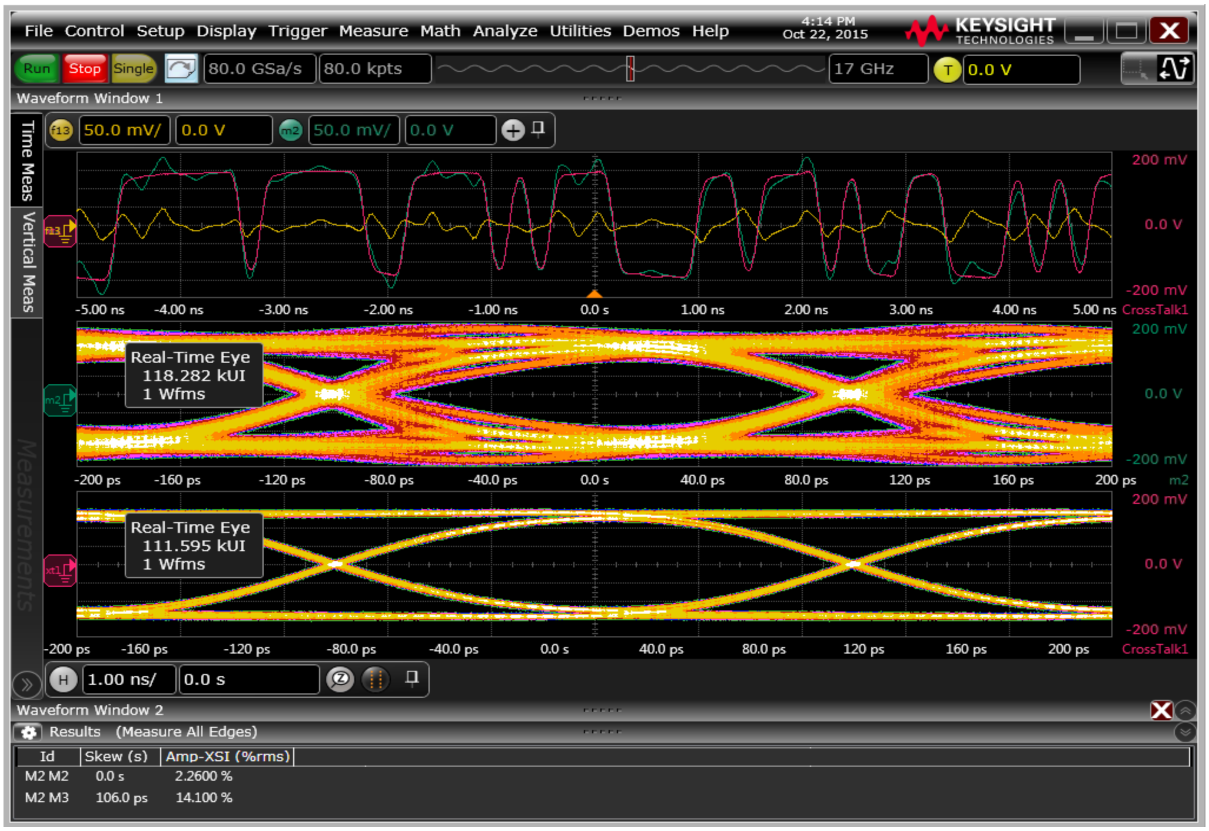
Examples of crosstalk analysis results

1. Transmission line crosstalk result example

Figure 10 shows the victim and aggressor waveforms (in green and orange) in the top plot along with the crosstalk-removed waveform in red. The middle plot shows the eye diagram of the victim waveform with the tall crosstalk peak or bulging on the left side of the eye indicative of FEXT. The bottom plot shows the eye diagram for the crosstalk-removed waveform.

In this particular example, the crosstalk magnitude of the victim-aggressor (M2 M3, Amp-XSI (%rms)), which is the RMS value of the crosstalk divided by the RMS value of the measured waveform reported, shown at the bottom of the figure is 14%. The eye opening is significantly improved when the crosstalk is removed from the victim waveform.

The victim ISI magnitude (M2 M2, Amp-XSI (%rms) shows about 2%, and it is not a significant contributor to the victim waveform distortion.



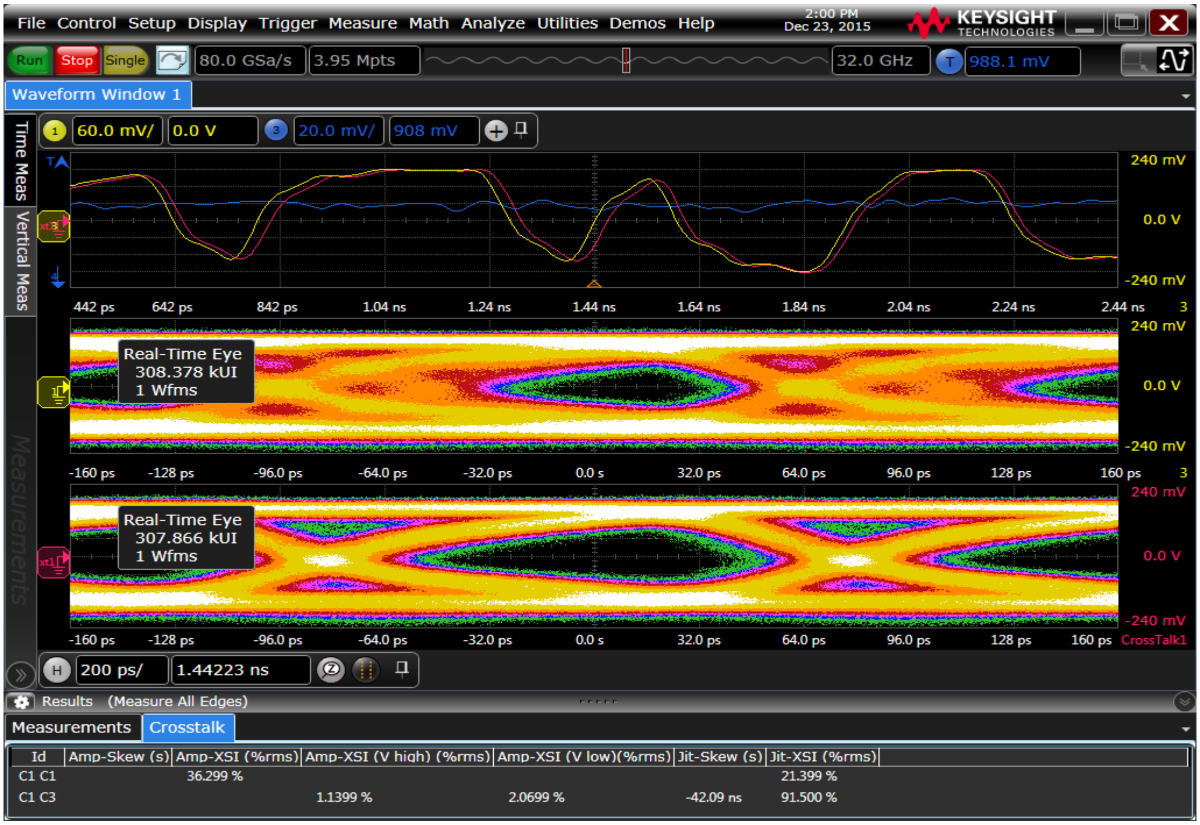
Id	Skew (s)	Amp-XSI (%rms)
M2 M2	0.0 s	2.2600 %
M2 M3	106.0 ps	14.100 %

Figure 10. Before and after view of a victim waveform with FEXT. The top plot shows the victim waveform in green, the aggressor in orange, and the crosstalk removed waveform in red. The middle plot is the eye diagram of the victim with the bulging indicative of FEXT, and the bottom plot is the eye diagram of the victim after removing crosstalk.

2. Power supply aggressor crosstalk result example

The following example illustrates the effect a noisy power supply can have on the jitter of a serial data signal. Figure 11 shows the serial data victim and power supply aggressor waveforms (in yellow and blue) in the top grid along with the crosstalk-removed waveform in red. The power supply is creating excessive jitter on the victim, as seen in the upper eye diagram. In this case, the perturbations in the power supply change quite slowly relative to the data signal's unit interval, but by scrolling through the waveform, you can see that as the power supply increases in voltage, the data signal is delayed in time. As the power supply decreases in voltage, the data signal advances in time. In this example, the application created a model for the jitter in the data signal that is attributed directly to the voltage variation of the power supply and removed that crosstalk error from the victim in the lower eye diagram. The eye diagram of the crosstalk-removed waveform at the bottom is considerably improved from the one above it, showing that the power supply aggressor was responsible for most of that jitter.

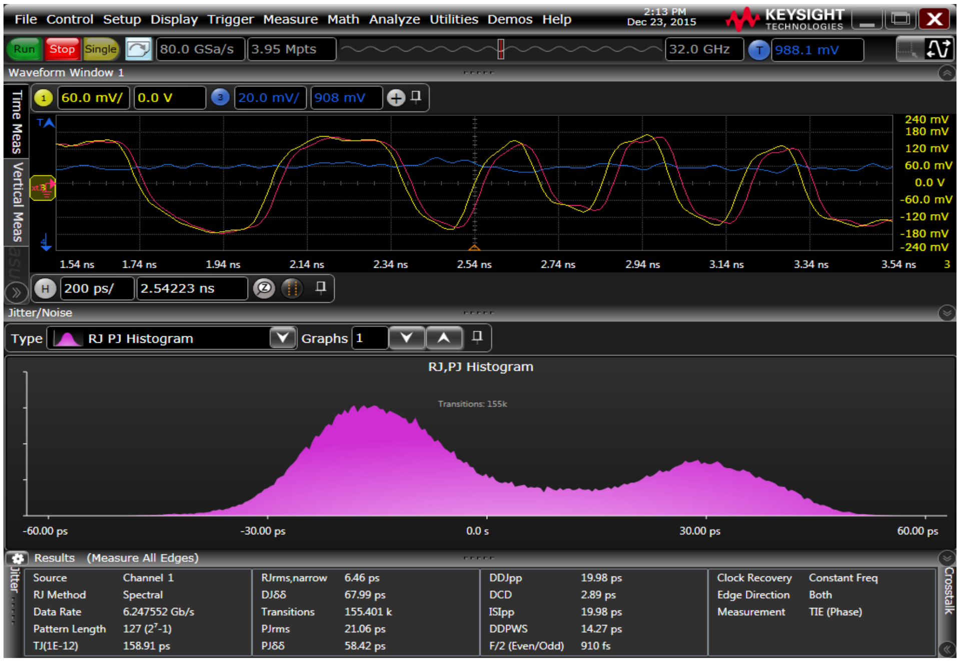
This particular example does not have a lot of amplitude crosstalk from the power supply, as shown by the low values of C1 C3, Amp-XSI (V high) and C1 C3, Amp-XSI (V low). These values represent the relative magnitudes of crosstalk distortion caused by the aggressor power supply on the serial data victim. There is, however, a significant amount of jitter in the data signals caused by the power supply, as shown by the large C1 C3, Jit-XSI value.



Id	Amp-Skew (s)	Amp-XSI (%rms)	Amp-XSI (V high) (%rms)	Amp-XSI (V low)(%rms)	Jit-Skew (s)	Jit-XSI (%rms)
C1 C1		36.299 %				21.399 %
C1 C3			1.1399 %	2.0699 %	-42.09 ns	91.500 %

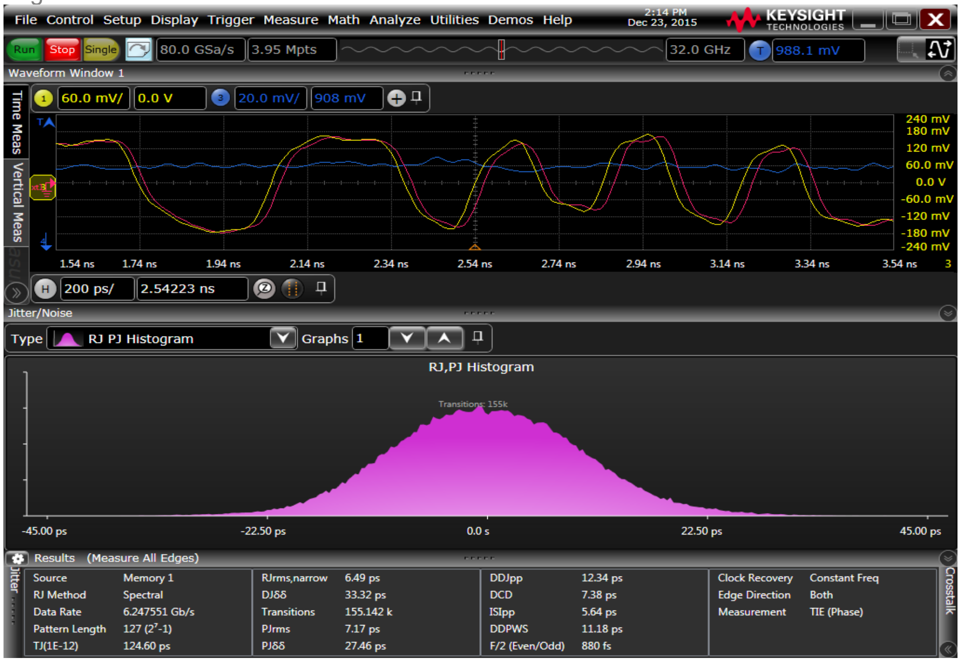
Figure 11. Crosstalk example of a power supply aggressor generating jitter on a serial data victim.

Taking the analysis a step further, EZJIT Plus can be used to quantify the timing improvement by comparing the jitter statistics of the before and after waveforms. Figure 12 shows a capture of the RJPJ histogram (bottom) for the original serial data waveform. The power supply has a strong periodic component that is showing up primarily as a large PJdd value in the jitter statistics (at the very bottom). The large PJdd value also creates large PJrms and DJdd values. Figure 13 shows the same results for the crosstalk-removed waveform. Note the improvement in the RJPJ histogram and the large reduction in PJdd, and related statistics, such as DJdd and PJrms.



Source	Channel 1	RJrms,narrow	6.46 ps	DDJpp	19.98 ps	Clock Recovery	Constant Freq
RJ Method	Spectral	DJδδ	67.99 ps	DCD	2.89 ps	Edge Direction	Both
Data Rate	6.247552 Gb/s	Transitions	155.401 k	ISIpp	19.98 ps	Measurement	TIE (Phase)
Pattern Length	127 (2^7-1)	PJrms	21.06 ps	DDPWS	14.27 ps		
TJ(1E-12)	158.91 ps	PJδδ	58.42 ps	F/2 (Even/Odd)	910 fs		

Figure 12. Jitter analysis results using EZJIT, showing the large amount of jitter in the original serial data waveform.

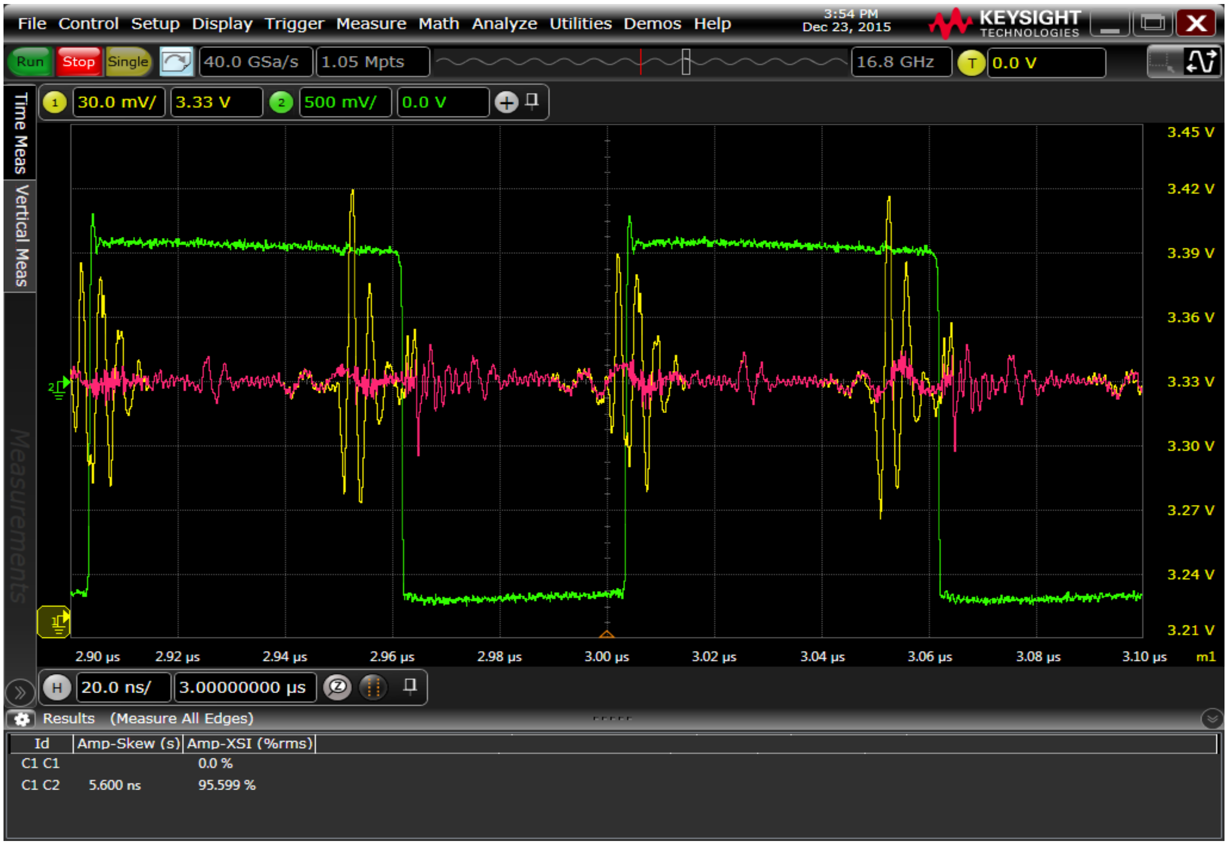


Source	Memory 1	RJrms,narrow	6.49 ps	DDJpp	12.34 ps	Clock Recovery	Constant Freq
RJ Method	Spectral	DJδδ	33.32 ps	DCD	7.38 ps	Edge Direction	Both
Data Rate	6.247551 Gb/s	Transitions	155.142 k	ISIpp	5.64 ps	Measurement	TIE (Phase)
Pattern Length	127 (2^7-1)	PJrms	7.17 ps	DDPWS	11.18 ps		
TJ(1E-12)	124.60 ps	PJδδ	27.46 ps	F/2 (Even/Odd)	880 fs		

Figure 13. Jitter analysis results using EZJIT, demonstrating the improvement in jitter statistics after removing the jitter generated by the power supply.

3. Power supply victim crosstalk result example

This example demonstrates the crosstalk analysis application’s ability to identify any crosstalk corruption of a power supply. Although this example uses the Vcc rail, the methods and results can apply to either supply rail. Figure 8 shows a power supply waveform (in yellow) that is a victim of crosstalk from a clock signal aggressor (in green). Note the large ringing in the power supply that is correlated with the edges of the clock. The red signal is the power supply signal after removing the crosstalk generated by the clock edges. The ringing has been removed. The crosstalk magnitude of the victim-aggressor (C1 C2, Amp-XSI), which is the RMS value of the crosstalk divided by the RMS value of the measured waveform reported, shown at the bottom of the figure is more than 95%, which indicates a strong correlation of the clock edges aggressing at the power supply.

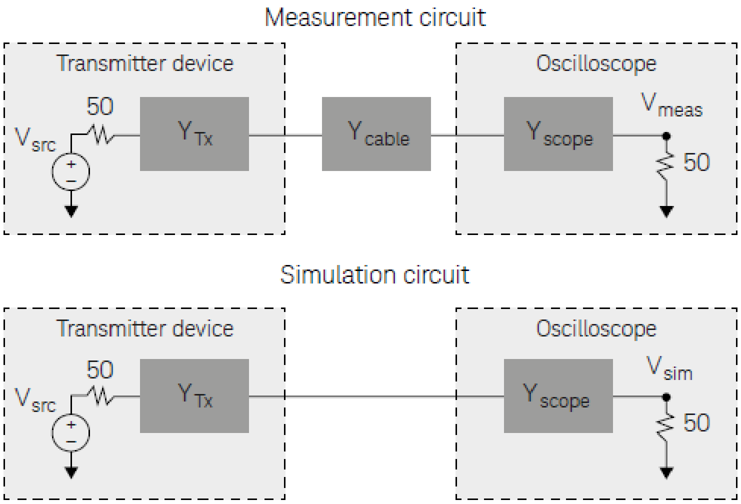


Id	Amp-Skew (s)	Amp-XSI (%rms)
C1 C1		0.0 %
C1 C2	5.600 ns	95.599 %

Figure 14. Example of a power supply being treated as a victim. Victim waveform (yellow), aggressor (green) and crosstalk-removed waveform (red).

InfiniiSim

What is InfiniiSim?



InfiniiSim has two modes: Basic and Advanced. Basic is available in D9010DMBA, Advanced is available in D9020ASIA. Advanced has all capabilities of Basic, and more. This document will describe the features of both, with notes telling you if the feature is Advanced only. If you only need Basic mode, and have no need for equalization or crosstalk analysis, consider D9010DMBA instead.

InfiniiSim works by relating the transfer functions of two circuits to yield an overall transfer function between them. The two circuits (the 'measurement circuit' and 'simulation circuit') are defined by the user. The measurement circuit represents the measurement setup the user has on the bench, while the simulation circuit represents the circuit the user would like have. As an example, the measurement circuit shown in Figure 1 comprehends a source device being measured by an oscilloscope with a cable in between.

The simulation circuit has the cable removed. By relating the observation points in both circuits (the same location in this instance) to the source voltage, an overall transfer function that removes the effects of the cable results.

For the measurement circuit: $H_m(f) = \frac{V_{meas}(f)}{V_{src}(f)}$

For the simulation circuit: $H_s(f) = \frac{V_{sim}(f)}{V_{src}(f)}$

Relating the two to create the overall transfer function: $H(f) = \frac{H_s(f)}{H_m(f)} = \frac{V_{sim}(f)/V_{src}(f)}{V_{meas}(f)/V_{src}(f)} = \frac{V_{sim}(f)}{V_{meas}(f)}$

Such that: $V_{meas}(f) * H(f) = V_{sim}(f)$

We now have a simulation result that indicates the measurement we would get if the cable was removed. This example is the simplest case that InfiniiSim handles. More blocks can be used in the simulations and other observation points considered.

Common use models for productivity

InfiniiSim works by relating the transfer functions of two circuits to yield an overall transfer function between them. The two circuits (the ‘measurement circuit’ and ‘simulation circuit’) are defined by the user. The measurement circuit represents the measurement setup the user has on the bench, while the simulation circuit represents the circuit the user would like have. As an example, the measurement circuit shown in Figure 1 comprehends a source device being measured by an oscilloscope with a cable in between.

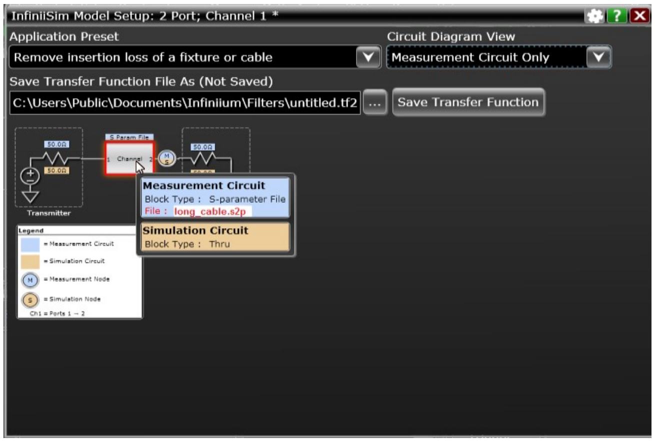
1. **Removal of channel element insertion loss**: One block of loss such as from a cable or fixture between a digital source and the oscilloscope. The inverse gain of the block (S21-1) is determined and its time response is convolved with the acquisition.
2. **Inserting a channel element insertion loss**: One block of loss such as from a standard cable model to be inserted before the oscilloscope. The S21 of the block is determined and its time response is convolved with the acquisition.
3. **Remove scope input reflection (Advanced only):** Modeled using two blocks - one for the transmitter source and the other for the oscilloscope input (so the oscilloscope input reflection can be removed)
4. **Remove all effects of a channel element (Advanced only):** Using S-parameter models of source and scope load, the effects of a channel element are totally removed. This is different from 1 above (removing insertion loss) in that the interactions between the elements are taken into account. This provides the most accurate way to remove a channel element.
5. **Add all effects of a channel element (Advanced only):** Using S-parameter models of source and scope load with, a complete insertion of a channel element is performed. This is different from the Inserting a channel element insertion loss (#2 above) in that the reflective interactions between the elements are taken into account. This provides the most accurate rendering to insert a channel element such as a standard cable.
6. **Replace one channel element with another (Advanced only):** Modeled after removing or adding all effects of a channel element, one channel element block is easily substituted for another. Interactions between transmitter and oscilloscope elements are taken into account.
7. **Measurement plane relocation (Advanced only):** Measurement plane relocation allows you to view any voltage waveform in a circuit as the circuit exists by moving the simulation node to any location you desire. This is an ‘in situ’ analysis so is not a ‘removal’ or ‘insertion’ viewpoint.
8. **Relocate the observation node of a probed measurement (Advanced only):** View any voltage waveform in the probed circuit as the circuit exists by moving the simulation node to any location you desire. This is an ‘in situ’ analysis so it is not a ‘removal’ or ‘insertion’ viewpoint.
9. **Remove loading effects of oscilloscope probe (Advanced only):** To remove the loading effects of a probe, a topology of circuit blocks is given that allows probe models to be considered in the measurement. An oscilloscope probe, while it might be defined as ‘high impedance’, really does have a loading effect on the circuit. This effect can be taken into account and removed.
10. **Remove loading effects of a DDR interposer and probe (Advanced only):** To remove the effects of an interposer board in validating a dual data (DDR) memory system where the signals of the ball grid array (BGA) are not exposed and are unavailable for direct probing.
11. **General purpose configuration (Advanced only):** General topologies are provided for greater flexibility. General purpose probe, 6 block, and 9 block topologies are available with user defined measurement and simulation points and each block can be defined as having combinations of up to three elements in cascade or parallel arrangement so 27 total circuit elements can be defined for the most sophisticated scenarios.

Model your system as detailed as you need

InfiniiSim waveform transformation toolset offers a wide breadth of possibilities to suit your goals:

One block for simplest path compensation

Often you will simply want to compensate for the loss of a channel element, such as a cable or fixture. The one block model shown right gets this job done. It can also be extended to a remove/replace operation by changing simulation parameters. This is available in Basic and Advanced versions.


InfiniiSim Model Setup: 2 Port; Channel 1 *

Application Preset: Remove insertion loss of a fixture or cable

Circuit Diagram View: Measurement Circuit Only

Save Transfer Function File As (Not Saved): C:\Users\Public\Documents\Infiniium\Filters\untitled.tf2

Measurement Circuit
Block Type : S-parameter File
File : long_cable.s2p

Simulation Circuit
Block Type : Thru

Figure 2. One block channel element removal

Three-block analysis for true channel element removal and insertion

When the most precision is required for a single channel element removal and insertion is required you will need at least the 3 block model (Advanced only). This model uses block descriptions for the transmitter and the oscilloscope as well as the channel to describe the full system. The inclusion of the transmitter and oscilloscope blocks enable most complete waveform rendering by including the reflective S-parameter elements in the mathematical calculation of the transfer function used to transform from the measurement, M to the simulated measurement, S.

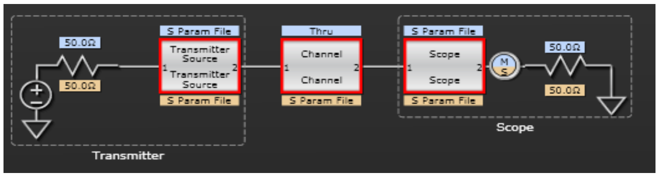


Figure 3. Three-block analysis for channel element insertion.

General purpose configurations

The InfiniiSim waveform transformation toolset includes three general purpose topologies to enable detail tailoring of the description of your circuit. For probe modeling, the general-purpose probe topology is used while for SMA differential probe usage, the general purpose 6 block model will find use in a majority of cases. For those very sophisticated applications, possibly using both high impedance probes and differential SMA probe heads, the general-purpose model can be used to describe these complex scenarios. One block analysis is available on Basic, while two or more blocks requires Advanced.

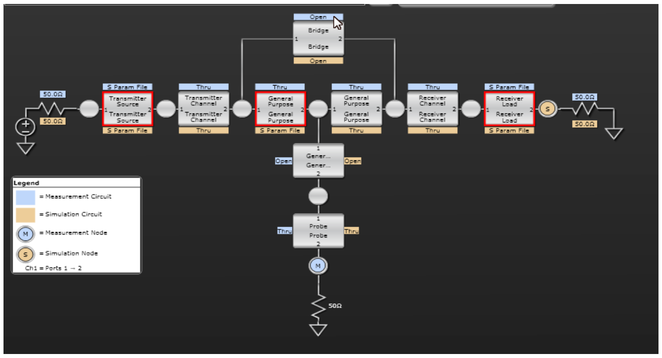
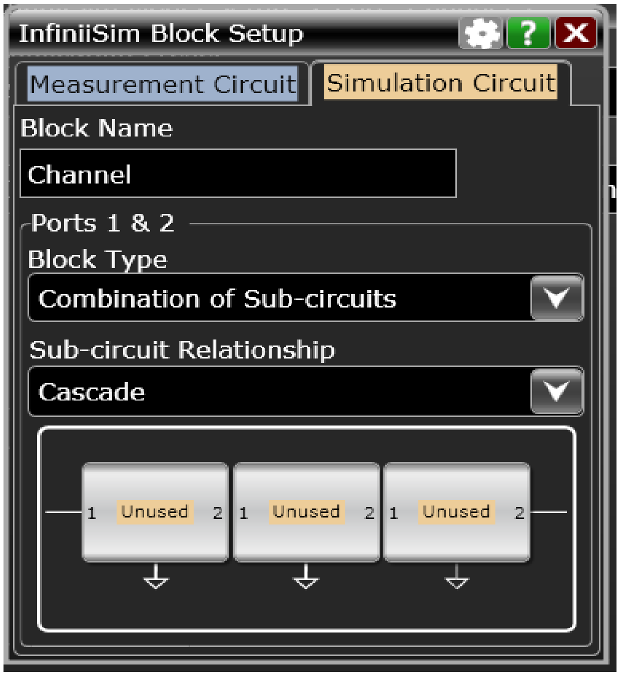


Figure 4. InfiniiSim can handle the most sophisticated system configurations with the general purpose 9-block configuration shown above.

Circuit models to define your setup (Advanced only)

The InfiniiSim waveform transformation toolset provides a graphical user interface for you to define your system as you understand it and can be almost arbitrarily complex. This is accomplished through topology selection and circuit block definition. The most common circuit block definition is that of an S-parameter model which can be measured directly using a vector network analyzer, be derived from a time domain reflectometer with appropriate conversion software or be created from a simulation tool such as the Advanced Design System.

S-Parameters can be entered as two port models (.s2p files) or as 4 port models (.s4p files). Circuit descriptions such as R-L-C definition or 'open' and 'thru' are also available as are more complex blocks that result from cascaded or parallel combinations of circuit elements. The InfiniiSim waveform transformation software makes AC small signal linearity assumptions to derive transfer functions from an actual measured location (node) to another location that where you aim to simulate measurement. This location may physically exist (but not be probable), or may incorporate a circuit model not actually present. The transfer function is used to derive a time domain 'filter' that is convolved with the acquisition to transform the acquired waveform to a waveform at the desired location.



InfiniiSim Block Setup

Measurement Circuit | Simulation Circuit

Block Name

Channel

Ports 1 & 2

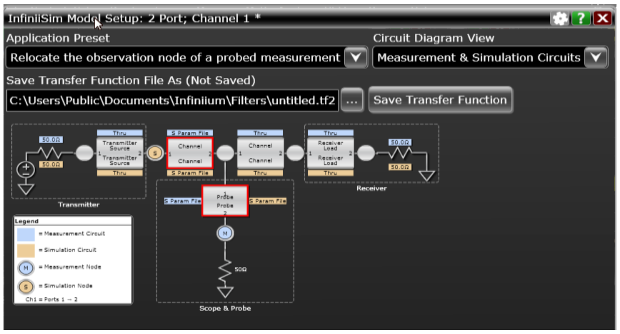
Block Type

Combination of Sub-circuits

Sub-circuit Relationship

Cascade

Figure 5. Sub-circuit capability: Any given InfiniiSim standard block can be described as a combination of sub-circuits.



InfiniiSim Model Setup: 2 Port; Channel 1 *

Application Preset: Relocate the observation node of a probed measurement

Circuit Diagram View: Measurement & Simulation Circuits

Save Transfer Function File As (Not Saved)

C:\Users\Public\Documents\Infiniium\Filters\untitled.tf2

Figure 6. Measurement and Simulation circuits. Blue designates the measurement circuit elements while the brown labeling designates the simulation circuit elements.

Measurement and simulation circuits (Advanced only)

The core of the InfiniiSim waveform transformation software is in defining two circuits: one that defines your measurement setup and the other to define what you desire to have as your measurement. The first we call the 'measurement circuit' and the second is the 'simulation circuit'. These can be as simple as one block between the source and the oscilloscope load, or as complex as nine circuit blocks as in general purpose model. The simulation and measurement circuits share the topology selected, however, in many cases, circuit definitions for each block will be very different from measurement to simulation. This leads to great flexibility in transforming acquisitions at a measurement point to any other virtually probed location. For the circuit shown in Figure 6, for instance, Block `P' has an S parameter file describing its loading during measurement, however, for simulation, the loading is desired to be eliminated, thus the `open' designation.

See what you deserve to see

With the InfiniiSim waveform transformation toolset, you can see transformed signals in confidence whether channel elements are being inserted removed or whether the measurement plane is being relocated. Figure 7 shows a waveform of a digital signal at 1.8 Gb/s going through a combination of fixture and cable. Note that for the longer sequences of identical digits the waveform reaches a level that is very different from when the data changes frequently. This is called ISI and is seen when the channel exhibits low pass filter characteristics. The fixture and cables were measured with a 4-port Vector Network Analyzer and removed using the channel element removal selection in InfiniiSim. The yellow CH1 trace in Figure 7 depicts the results. Note the blue waveform depicting the 'before measurement' directly at the transmitter versus the yellow waveform transformed using the 4-port channel model of the fixture.

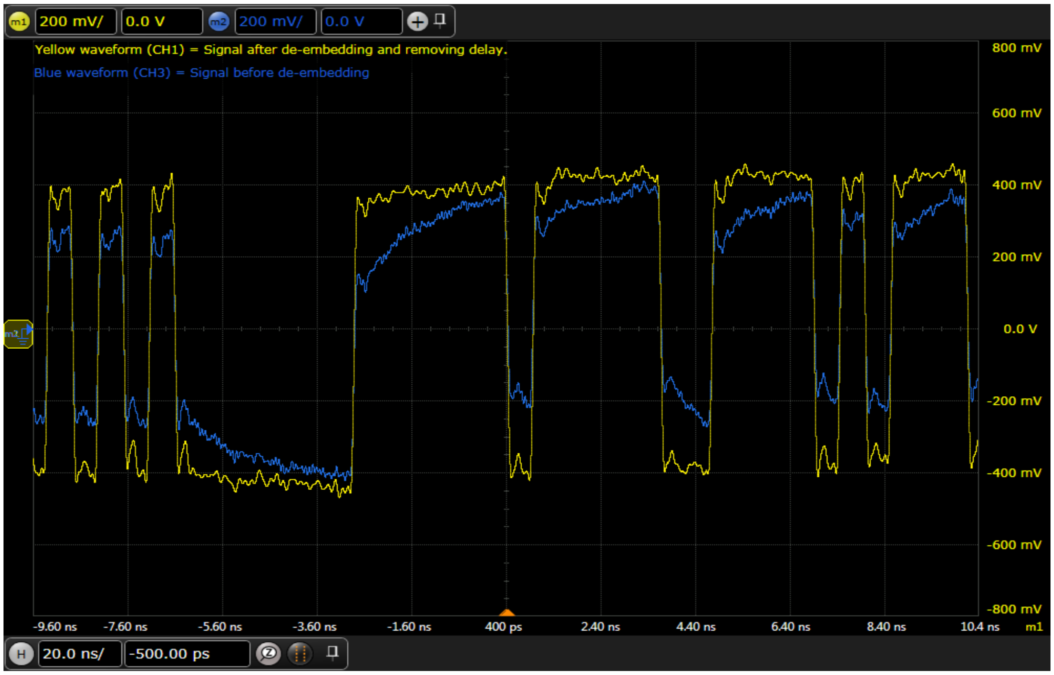


Figure 7. De-embedded, yellow, channel 1 waveform along with original channel 3 waveform.

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