DATA SHEET

D9040EDPV Embedded DisplayPort Electrical Performance Validation Software

The Keysight Technologies, Inc. eDP electrical performance and Validation (EPV) software for Infiniium Series oscilloscopes (see Ordering Information table below) provides you with a fast and easy way to verify and debug your eDP interface designs for embedded systems. The eDP Electrical Performance Validation software is designed to be uniquely flexible to handle the wide variety of configurations that are possible in embedded systems and pose characterization challenges. It offers the standard tests that are recommended as well as other informative tests, so it functions equally well as a validation tool. It displays the measurement data results in a flexible report format, and the report also provides a margin analysis that shows how closely your device passed or failed each test.

To make measurements with the eDP EPV software, you will also need an eDP TPA fixture for high-speed signal access as well as for AUX channel and other lines of the interface. Available fixtures are identified in the Test Accessories table below.

The eDP EPV software is based broadly on the widely-industry-accepted Keysight DisplayPort D9040DPPC compliance application, which extends utility to include a wizard graphic user interface that enables test selection, parameter election, test specification entry, and test template sharing. These features are unique in the industry and are supported to enable ecosystem sharing of test process specifics for highly variant embedded designs.

There is no official interoperability program for eDP, though this software goes a long way to create a defacto program – if only for a specific product or family of products. The default specifications are those found in the VESA[1] test guideline eDP PHY CTG v1.0. The tests available in the eDP EPV software package are identified in Table 1. However, there is no limit to what tests you can have available with the Infiniium framework add-in feature, with which you can add your own tests or tests from colleagues to the test suite offered. Details of the add-in capability are covered in the Extensibility section below.

[1] Video Electronics Standards Association (www.vesa.org)

Features

The eDP Electrical Performance Validation software offers new and unique capabilities as well as the standard features available with all Keysight Infiniium framework applications:

- Full physical layer testing of high-speed lanes
- Verification of link layer physical layer control
- Test status tracking
- Measurement process configurability
- Automated scope measurement setup
- Bit rate parameters: Nominal value of bit rate, number of bit rates and test line limit for frequency accuracy
- Level parameters: Nominal value of level, number of levels and test line limits for level accuracy or value of relative change between level settings
- Pre emphasis parameters: Nominal value of pre-emphasis, number of pre-emphasis settings and test line limits for pre-emphasis accuracy or value of relative change between pre-emphasis settings
- Eye diagram mask testing: Entry of arbitrary mask through mask files vs. bit rate
- Jitter testing: entry of arbitrary RJ, DJ, TJ values vs. bit rate
- Test plan creation: Selection of device conditions to test
- Test template: Create default templates for device types avoiding re-entry and share complete test process setup with others for consistent settings for same process requirements in different locations
- Test results reports with pass/fail margin analysis

With the eDP EPV test software, you can finally solve the myriad of test issues that embedded test systems present with one application.

Easy test process definition

The eDP Electrical Performance Validation software extends the ease-of-use advantages of Keysight's Infiniium Series oscilloscopes and previous DisplayPort standard test software to testing eDP designs.

The application will guide you through device setup and test connection with setup wizards to capture all the test process details. In doing so, you will create a tailored process to validate or characterize your device and get exactly what you need.

Using the eDP Electrical Performance Validation Software

The eDP application is started from the analyze tab in the Infiniium GUI. When selected and finished loading, the screen in Figure 1 is presented. This screen looks much like other applications in the Infiniium framework. Of particular note, after selecting the standard to test (eDP) and the test suite (High-Speed Physical Layer Tests) are the Device Definition and Test Setup buttons.

These are selected in progression, Device Definition first and then Test Setup. You can test with the device definition defaults (determined by the template the user can set) and with the connections defined without any further manipulations. You can proceed to Select Tests tab to select tests you want to run for the test session and continue to running tests.

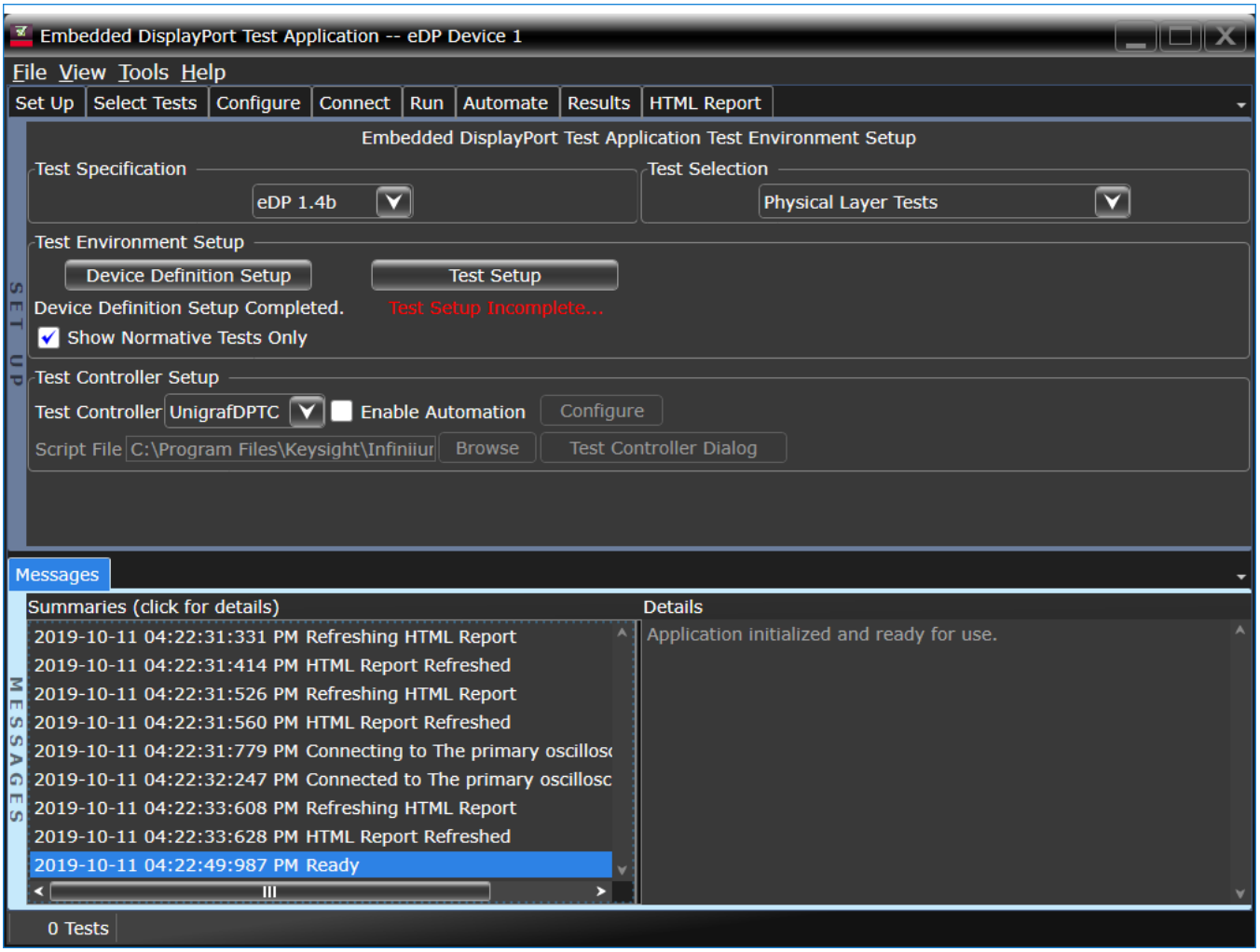


Figure 1. eDP test environment setup.

Device Definition

The Device Definition tab is where much of the eDP EPV software's power resides. When you click on the Device Definition Setup button, you will see a sequence of windows for you to define your device's capabilities and the specifications for these. You can see in Figure 2 how much information is shown in the second tab, Link Rate.

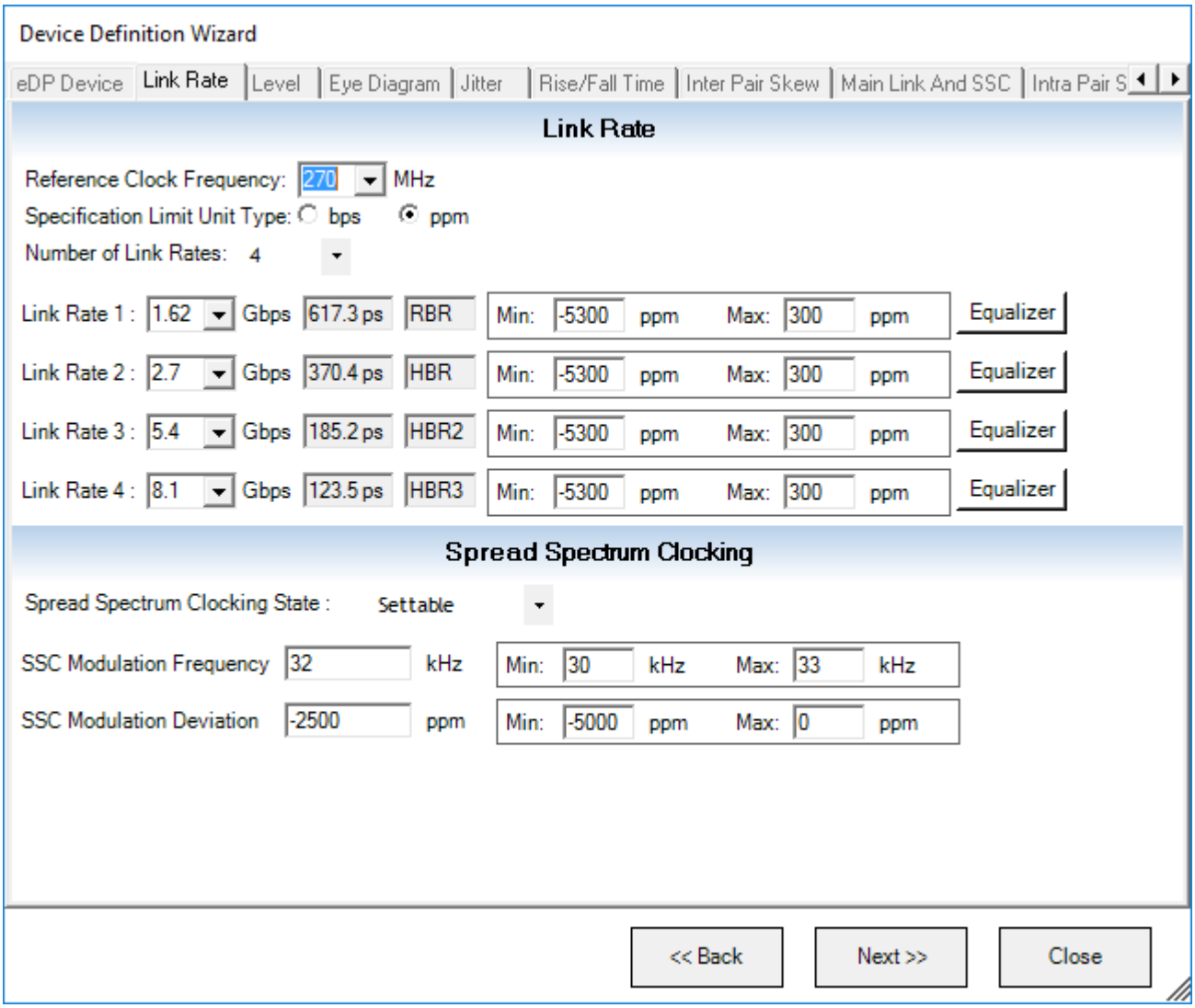


Figure 2. Link rate tab in Device Definition sequence

First, note that the tabs across the top of the window cover not only the device capabilities such as link rate and level but also capture the details necessary for all the tests that can be conducted. (Example: For eye diagram testing, you can set the pattern at which to test as well as the mask file to be used.)

The fundamental issues for eDP testing are addressed with this screen, and they are:
– The number of bit rates of which the device is capable.
– The nominal values of those bit rates.
– The manner to display the frequency accuracy of those bit rates: absolute error (bps) or ppm versus nominal link rate value. The minimum and maximum values are displayed for convenience.
– The CTLE (continuous time linear equalizer) attributes you want to use in the analysis measurements (eye diagram and jitter) to use for each bit rate.

These are defaulted to the values recommended in the VESA eDP standard but are easily alterable. Finally, since spread spectrum clocking (SSC) is a favored technique in embedded systems to keep EMI low, the SSC tests parameters and specifications are selectable here. It can be set to ‘Always On,’ ’Always Off,’ and ‘Settable.’

When the entries for the Link Rate window are complete, you will press ‘Next’ and proceed to the Eye Diagram and Jitter tabs to complete the product and test requirements. Figure 3 shows attributes of the Jitter tab and, at the same time, illustrates a very useful construct called Test Plan.’

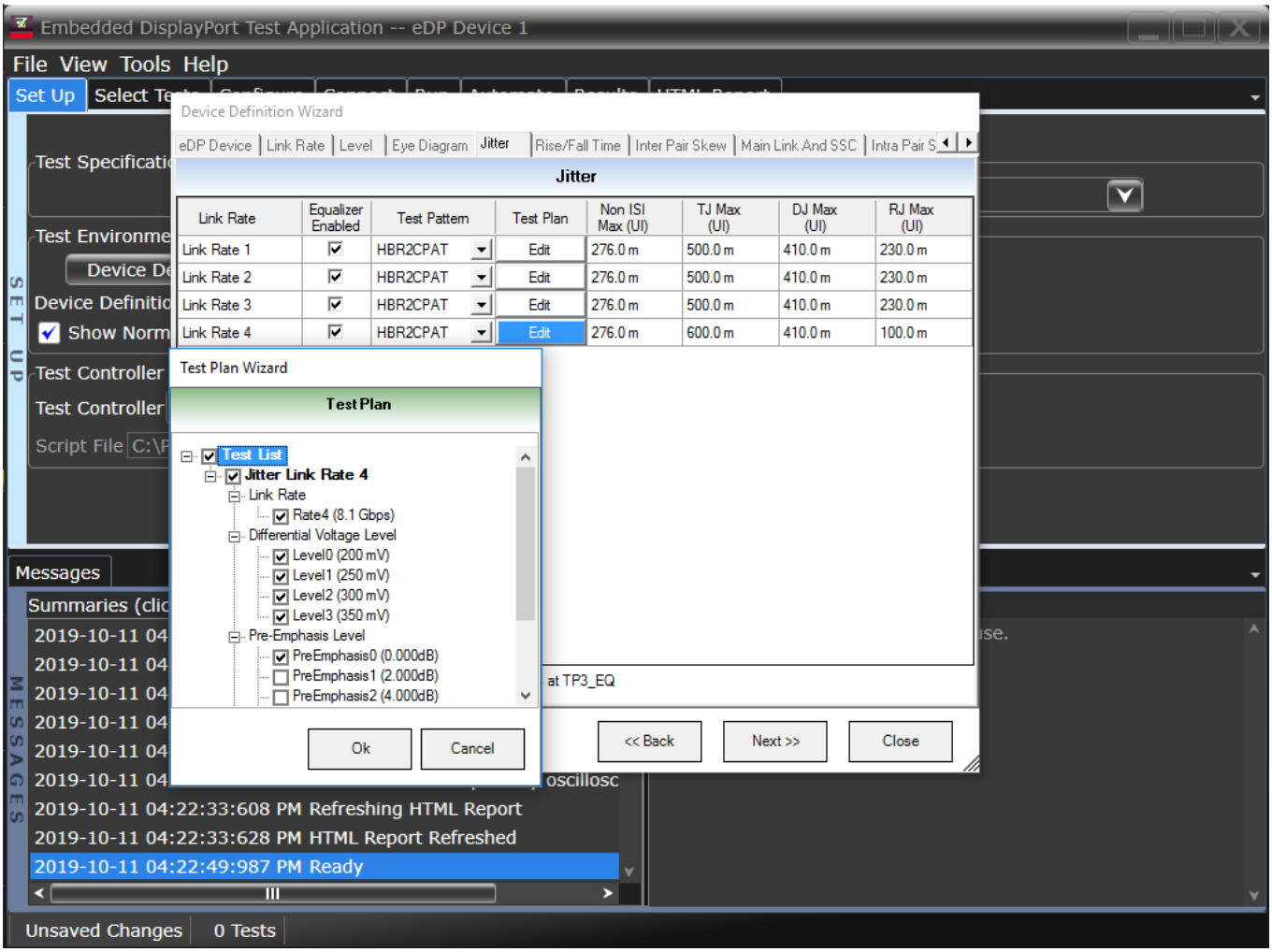


Figure 3. Jitter setup in the device definition sequence

In the Jitter Setup window, you will immediately see how comprehensive and flexible the software is. Firstly, it allows for all the link rates to be tested for jitter and allows for pattern type selection for the jitter measurement (selections are: PRBS7, HBR2CPAT, D10.2, random pattern). Then, you can enter the upper limits of jitter in the various components of jitter. Since the capability of your device includes different level settings and pre-emphasis settings, you might be interested in testing jitter for ALL combinations of these or just a few. By simply clicking the boxes in the Test Plan Wizard, you can select the device combinations to be tested.

When you have finished with the Jitter setup, you can save the setup as a template for the next time you test. Further, you can send this template to a colleague or partner so they can use the same setup, conditions and test line limits. You will see a status label below the Device Definition button, and you can click on this to select another template. At this time you now click the Test Setup button and Connection Setup button to enter the Test Session details: attributes of your work bench and test connection.

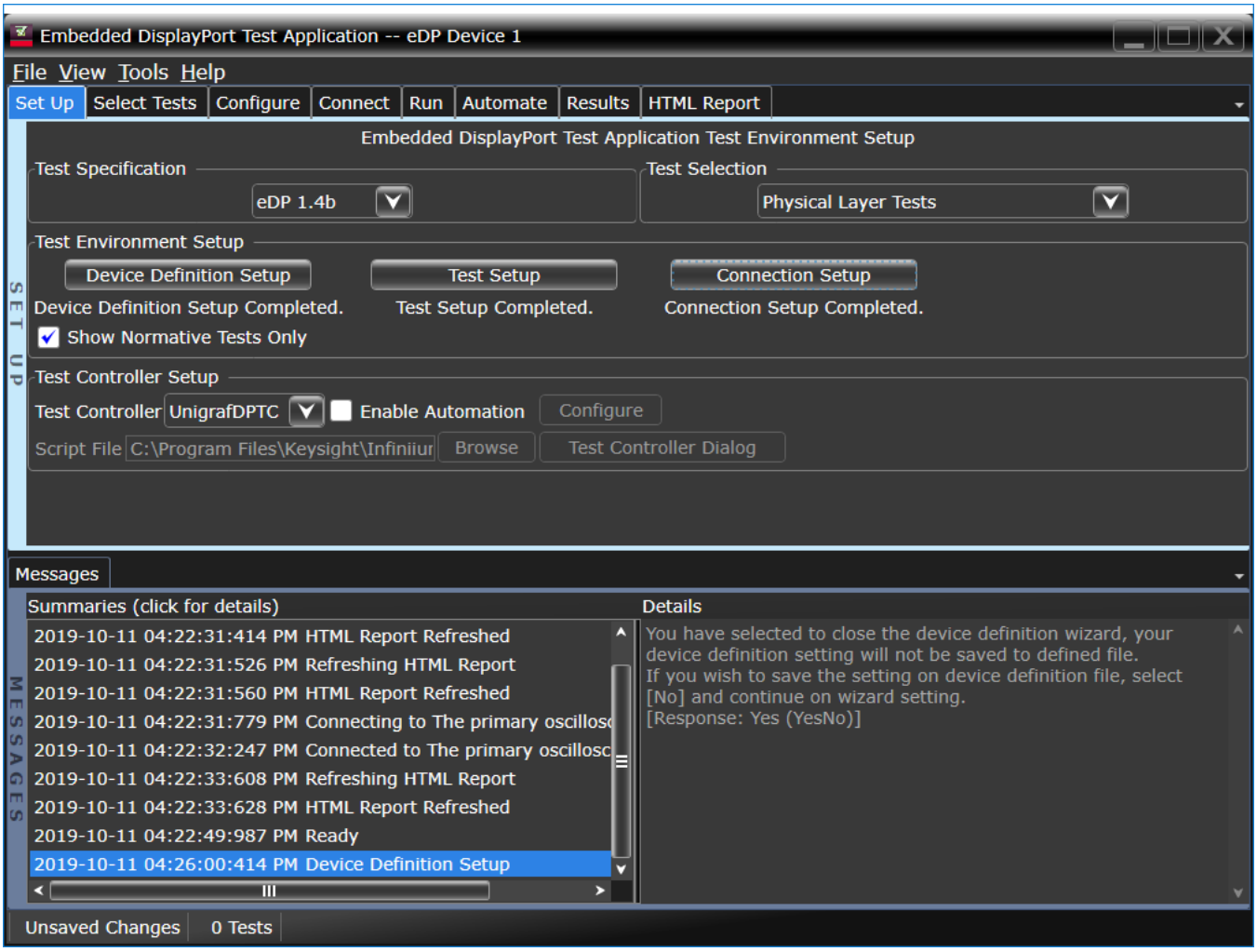


Figure 4. When finished with device setup, your specific template file is loaded.

Test Session

The eDP EPV test session wizard is leveraged from the DisplayPort test software wizard. Its purpose is to identify the connection to the oscilloscope and enable selecting the scope of testing for your current test session – say because of troubleshooting. For example, though a device might be defined in the Device Definition wizard, to have 4 bit rates and 4 lanes, you might be interested in only one lane and the eye diagram of one bit rate for a given experiment or characterization. The session test sequence is four screens, the purpose of which is to specify connection to the oscilloscope and to select only what you need for your immediate test objectives.

Test Setup

The Test Setup dialog allows you to narrow in on a specific lane, bit rate or level for a focused characterization test. The screen is shown below:

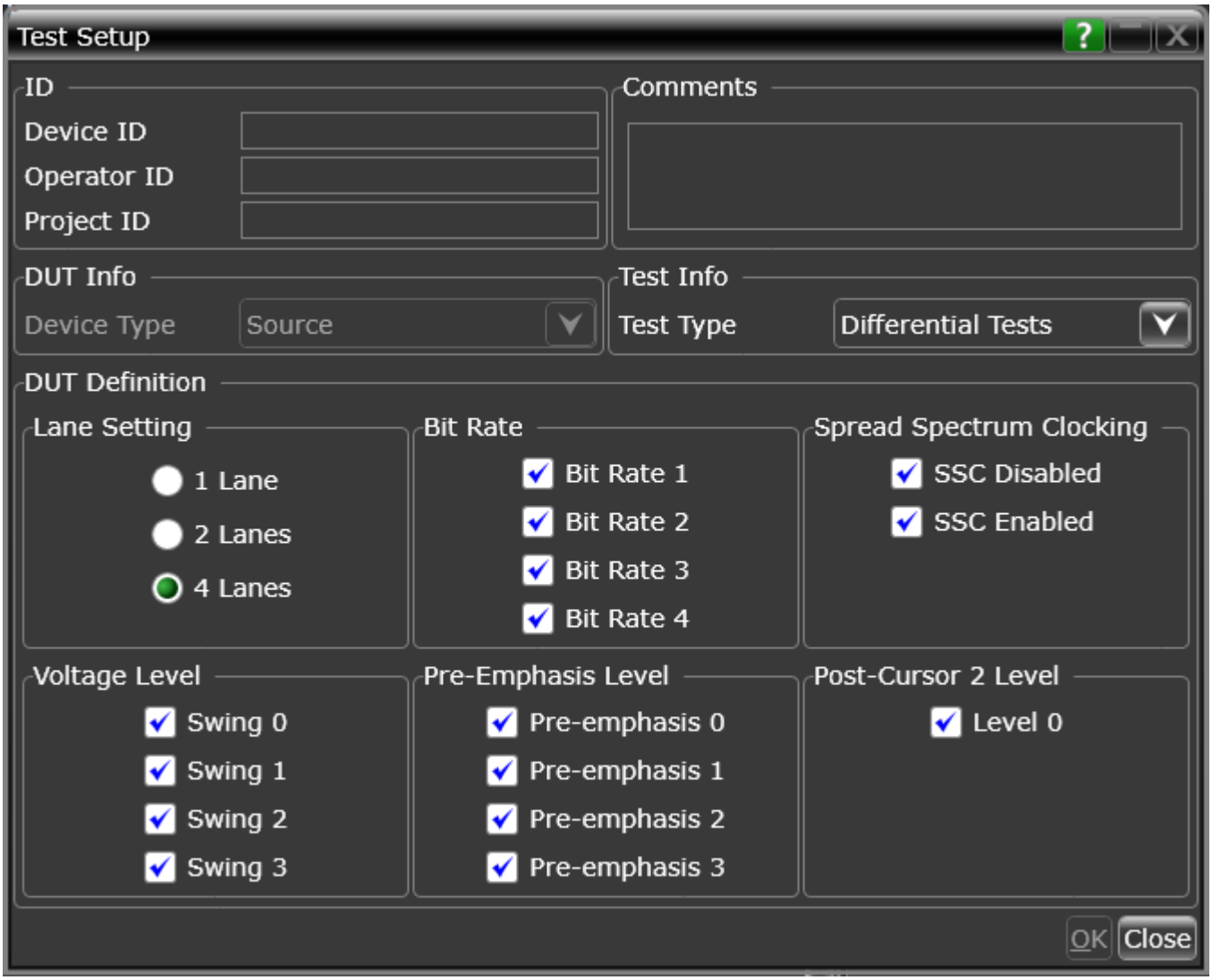


Figure 5. eDP session test details in setup.

You can select the specifics to test easily. For instance, if you just want to test 5.4 Gbs (bit rate 4), you would choose bit rate 4 and leave the other bit rates unselected. If you select all the bit rates for all the tests you selected in the test select tab, the software will run at all the bit rates you have selected.

Connection Setup

The Connection Setup dialog is the channel assignment setup. It will portray the connection expected in number of channels and type of connection requested. It is editable, and if there are channel assignment conflicts, the user is alerted to the fact. In a prior screen, you can select whether you want to use direct connection to the oscilloscope or connect with oscilloscope differential probes. Direct connection is recommended; however, using differential probe heads (SMA probe heads), you can connect four lanes simultaneously and measure all the differential tests in one test connection

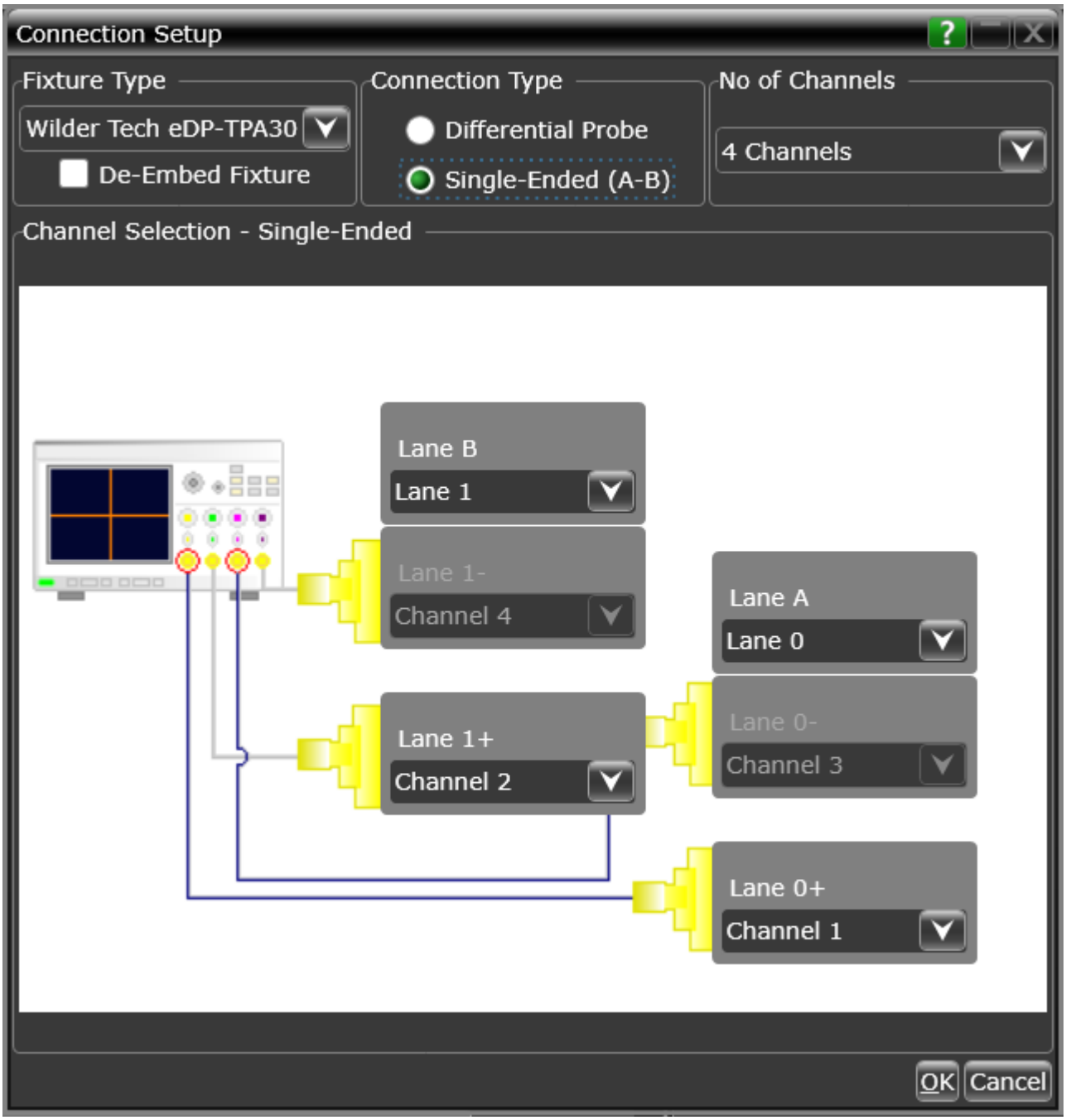


Figure 6. Channel assignment setup: lane and oscilloscope assignment: 2 lane single-ended connection using all four scope channels.

Test Selection

After defining the test environment through the Test Setup and Connection Setup, you are presented with only those tests that are appropriate for the device defined AND environment chosen. For example, if spread spectrum clocking (SSC) is not selected in the session description, then no SSC tests will appear; nor will they regardless of if the device definition setup defined the device to be SSC OFF only. A similar logic holds for pre-emphasis and levels as well. If your device definition is one lane only or defined device connection is one lane (one differential probe or two single-ended connections), then no inter-pair skew

tests will appear in the test suite. This dynamic filtering simplifies your job by ensuring you attempt to test only what is possible for the DUT and connection model you have chosen.

The eDP test suite is shown in the test selection screen (see Figure 7). It is partitioned in groups of tests as a function of the pattern that is required to test. By grouping them so, the number of required test interruptions is minimized. Shown is D10.2 (clock pattern), PRBS7 (127-bit repetitive pattern), and HBR2CPAT, which is a 2520-bit repeating pattern that was defined specifically for HBR2 in DisplayPort 1.2 – it is considered a key pattern to test with in most circumstances. Other patterns that may be used are PLTPAT (divide-by-10 clock) and random pattern, which is offered for flexibility.

Tests may be selected independently, and any number of tests may be selected for a given run. If more than one lane is possible to run (as determined by the selections in setup), then test selection by lane is also possible. If different connections or conditions of test are required from one test to another, a splash screen is presented to the user indicating the required change.

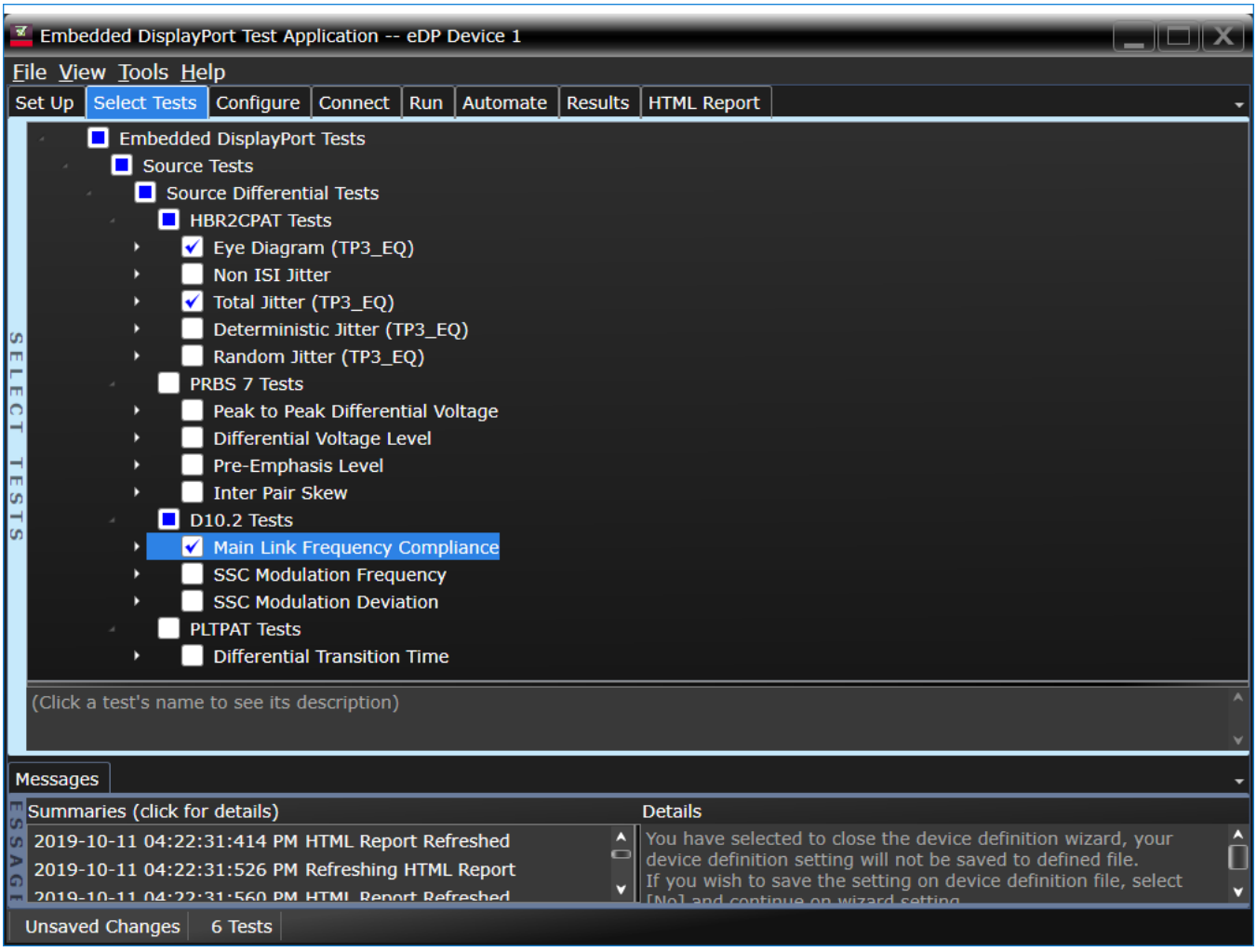


Figure 7. Lists the tests that are selectable and their status. Status bubbles indicate successful completion, failure or incompletion

Configurability and Guided Connection

The eDP Electrical Performance Validation software provides further flexibility in your test setup through the configure tab and will guide you to make connection changes with hookup diagrams when the tests you select require it.

While the most configurability is afforded in the test definition sequence, the configure tab allows for further possibility of modification of the test session operation for testing debug or ‘what-if’ analysis. For instance, you can alter transfer function, equalization or bandwidth of the measurement. In Figure 8, you can see some of the configurable parameters that can be altered in a given test session.

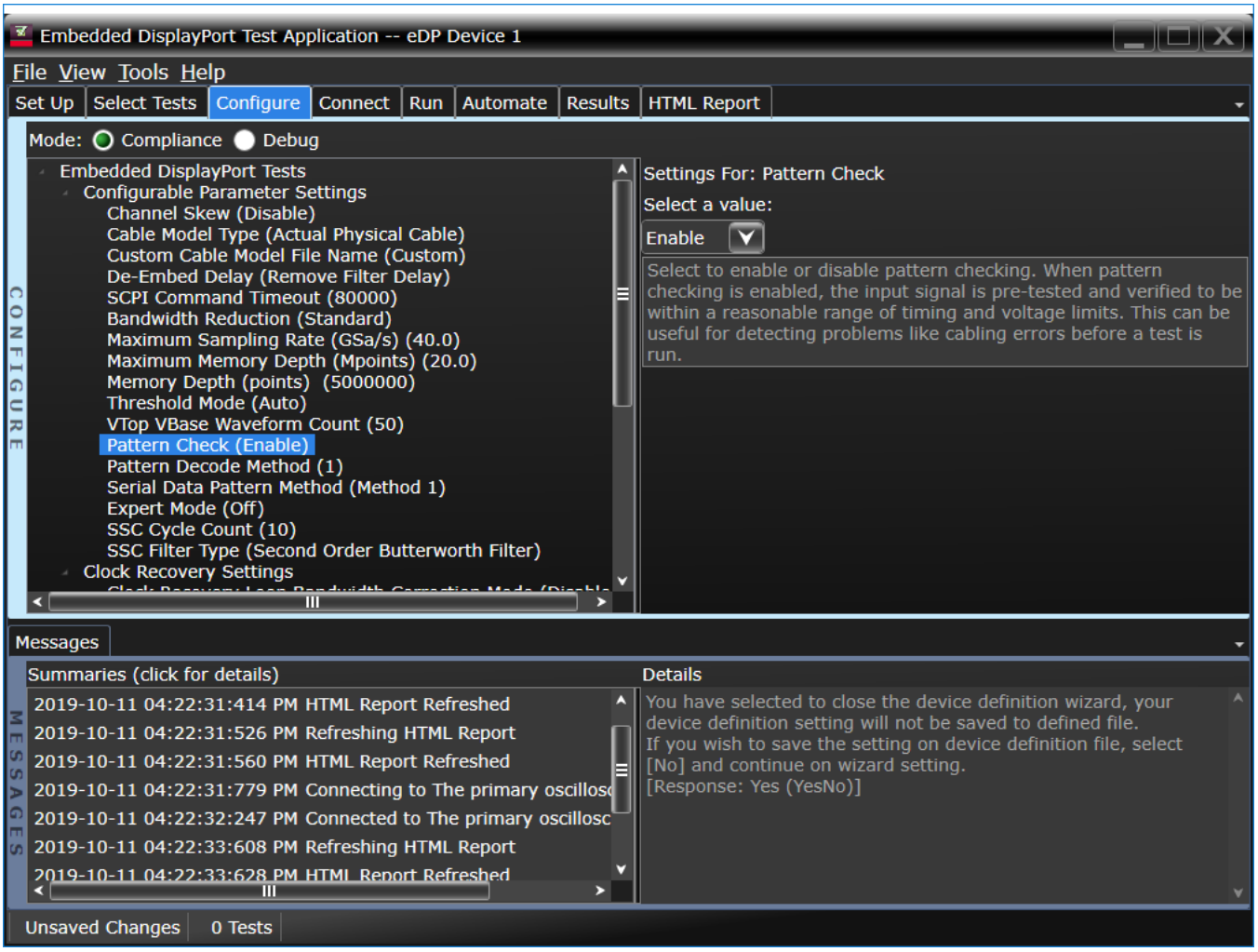


Figure 8. The eDP configure tab enables changing measurement parameters in the ‘Debug’ mode to support characterization and debug activities.

After you configure the test to meet your needs, the eDP EPV user interface displays the connection screen, which is specific to the configuration data you have selected. Figure 9 illustrates the typical connection guidance provided for a two-channel ‘A minus B’ connection model for a two lane test setup.

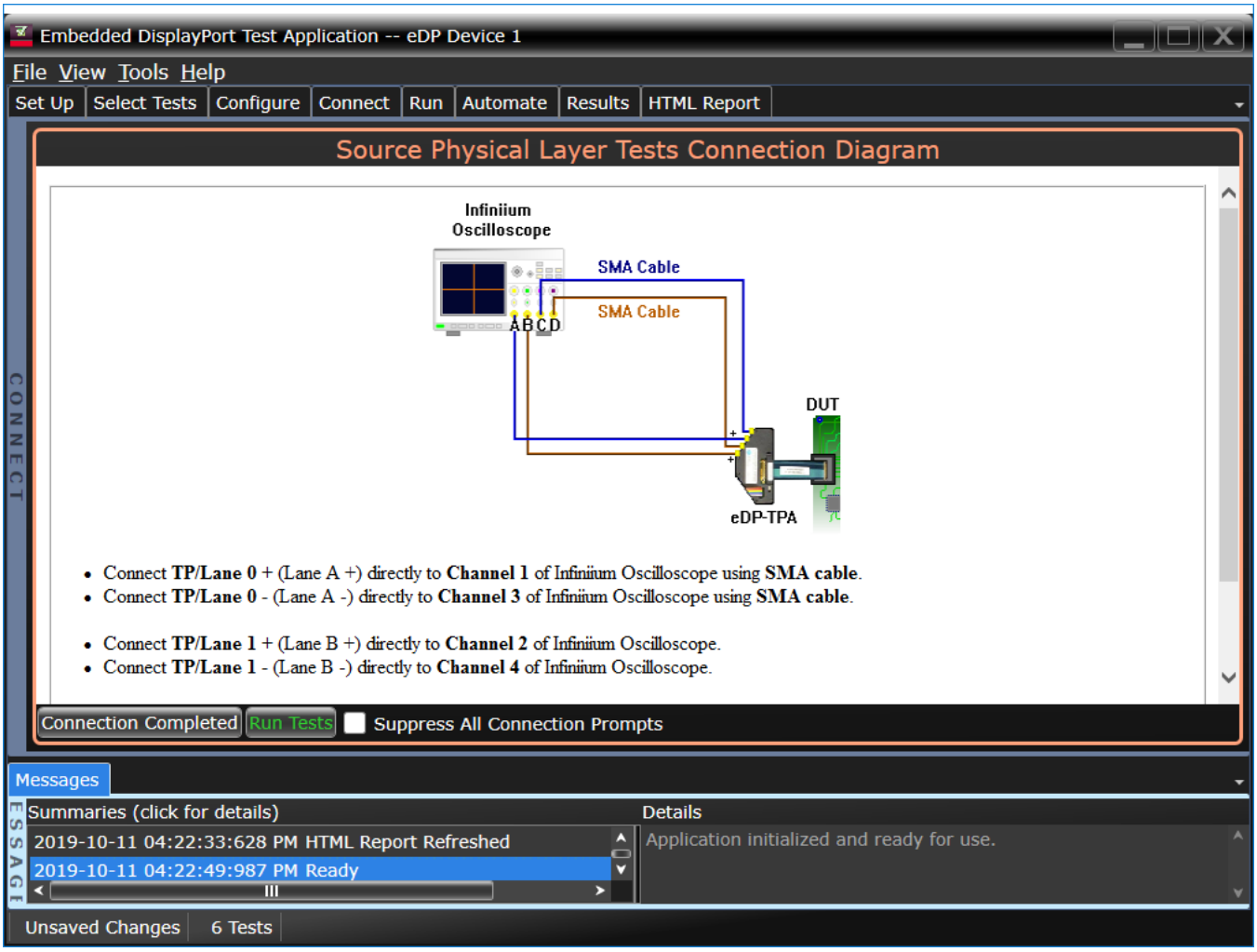


Figure 9. The final step before test is to illustrate the anticipated connection for the test.

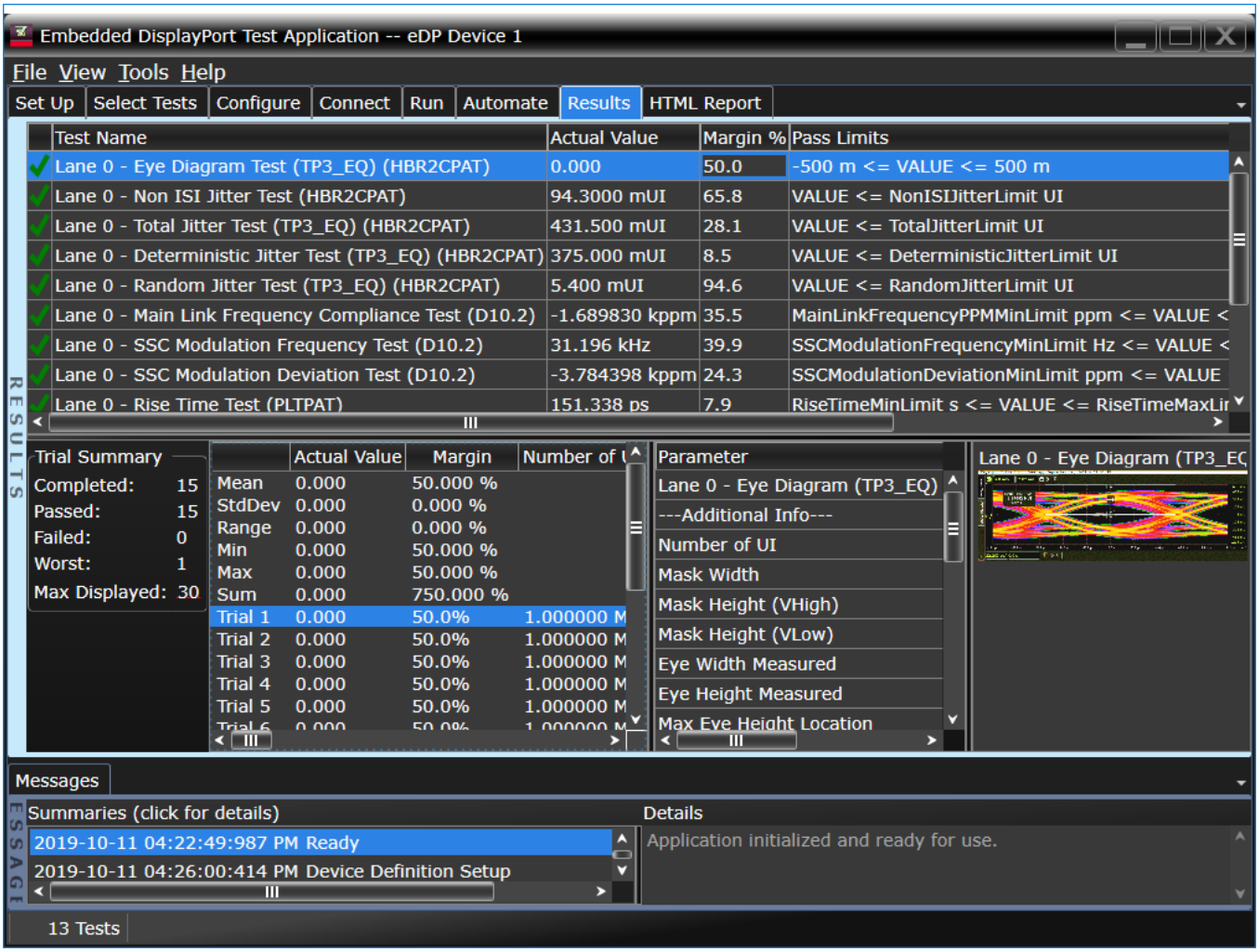
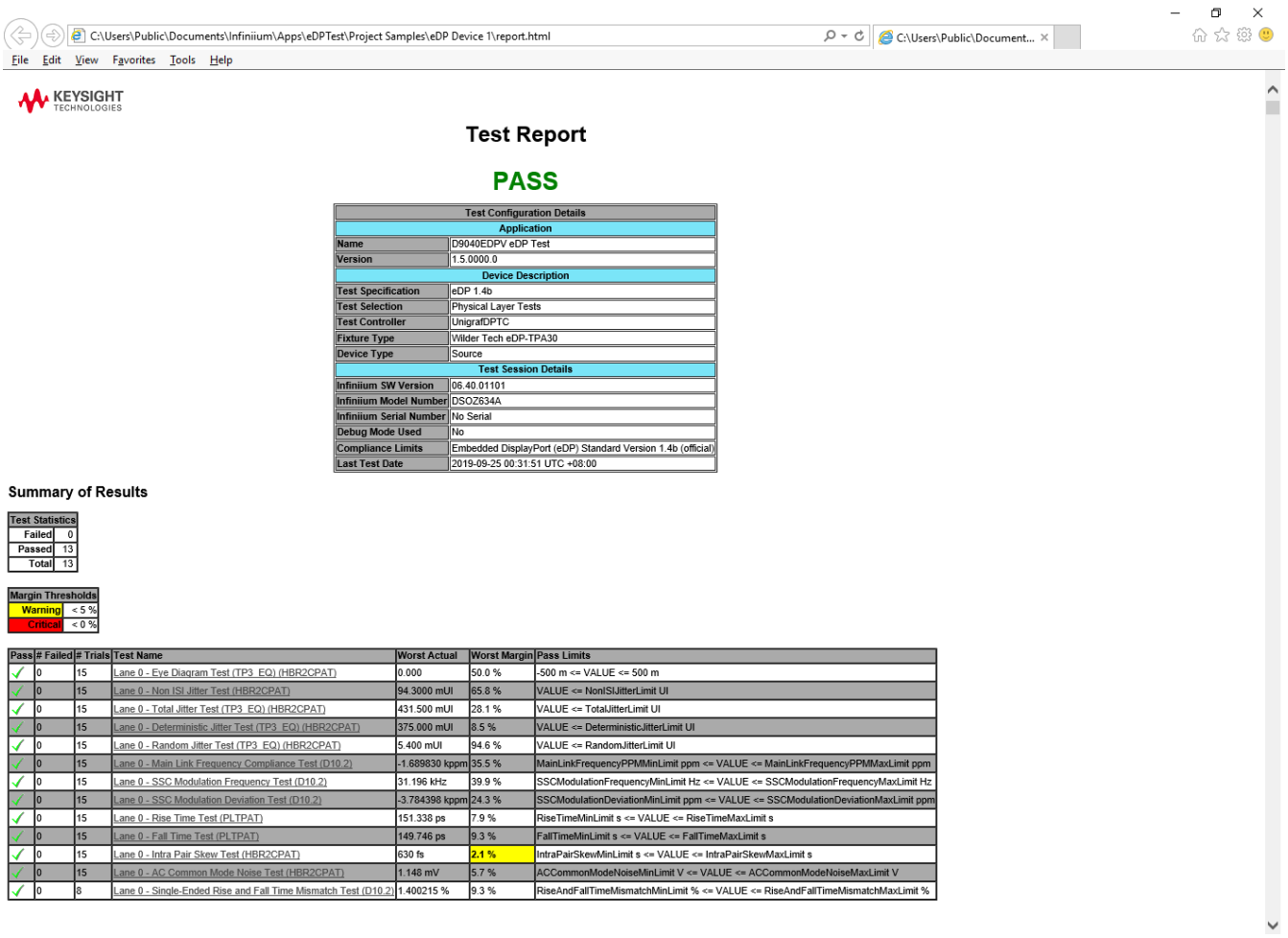


Figure 10. eDP EPV test software results report documents your test and indicates the pass/ fail status, test specification range, measured values and margin.

Thorough Performance Reporting

The eDP Electrical Performance Validation software generates thorough reports that not only capture the performance and status of the device under test, but also capture the screen shots of your most significant measurements for your perusal and evaluation. The first page of the report lists equipment and configuration details required in standard quality-assurance programs. It also provides a hot-linked results table that will quickly get you to the measurement report section of interest.



C:\Users\Public\Documents\Infiniium\Apps\eDPTest\Project Samples\eDP Device 1\report.html

File Edit View Favorites Tools Help

KEYSIGHT TECHNOLOGIES

Test Report

PASS

Test Configuration Details	
Application	
Name	D9040EDPV eDP Test
Version	1.5.0000.0
Device Description	
Test Specification	eDP 1.4b
Test Selection	Physical Layer Tests
Test Controller	UnigrafDPTC
Fixture Type	Wilder Tech eDP-TPA30
Device Type	Source
Test Session Details	
Infiniium SW Version	06.40.01101
Infiniium Model Number	DSOZ634A
Infiniium Serial Number	No Serial
Debug Mode Used	No
Compliance Limits	Embedded DisplayPort (eDP) Standard Version 1.4b (official)
Last Test Date	2019-09-25 00:31:51 UTC +08:00

Summary of Results

Test Statistics	
Failed	0
Passed	13
Total	13

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Worst Actual	Worst Margin	Pass Limits
✓	0	15	Lane 0 - Eye Diagram Test (TP3_EQ) (HBR2CPAT)	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	15	Lane 0 - Non ISI Jitter Test (HBR2CPAT)	94.3000 mUI	65.8 %	VALUE <= NonISIJitterLimit UI
✓	0	15	Lane 0 - Total Jitter Test (TP3_EQ) (HBR2CPAT)	431.500 mUI	28.1 %	VALUE <= TotalJitterLimit UI
✓	0	15	Lane 0 - Deterministic Jitter Test (TP3_EQ) (HBR2CPAT)	375.000 mUI	8.5 %	VALUE <= DeterministicJitterLimit UI
✓	0	15	Lane 0 - Random Jitter Test (TP3_EQ) (HBR2CPAT)	5.400 mUI	94.6 %	VALUE <= RandomJitterLimit UI
✓	0	15	Lane 0 - Main Link Frequency Compliance Test (D10.2)	-1.689830 kppm	35.5 %	MainLinkFrequencyPPMMinLimit ppm <= VALUE <= MainLinkFrequencyPPMMaxLimit ppm
✓	0	15	Lane 0 - SSC Modulation Frequency Test (D10.2)	31.196 kHz	39.9 %	SSCModulationFrequencyMinLimit Hz <= VALUE <= SSCModulationFrequencyMaxLimit Hz
✓	0	15	Lane 0 - SSC Modulation Deviation Test (D10.2)	-3.784398 kppm	24.3 %	SSCModulationDeviationMinLimit ppm <= VALUE <= SSCModulationDeviationMaxLimit ppm
✓	0	15	Lane 0 - Rise Time Test (PLTPAT)	151.338 ps	7.9 %	RiseTimeMinLimit s <= VALUE <= RiseTimeMaxLimit s
✓	0	15	Lane 0 - Fall Time Test (PLTPAT)	149.746 ps	9.3 %	FallTimeMinLimit s <= VALUE <= FallTimeMaxLimit s
✓	0	15	Lane 0 - Intra Pair Skew Test (HBR2CPAT)	630 fs	2.1 %	IntraPairSkewMinLimit s <= VALUE <= IntraPairSkewMaxLimit s
✓	0	15	Lane 0 - AC Common Mode Noise Test (HBR2CPAT)	1.148 mV	5.7 %	ACCommonModeNoiseMinLimit V <= VALUE <= ACCommonModeNoiseMaxLimit V
✓	0	8	Lane 0 - Single-Ended Rise and Fall Time Mismatch Test (D10.2)	1.400215 %	9.3 %	RiseAndFallTimeMismatchMinLimit % <= VALUE <= RiseAndFallTimeMismatchMaxLimit %

Figure 11. The eDP software generates a summary report where you can see the total test results for your device quickly and clearly. Additional details are available for each test, including the test limits, test description and test results, including waveforms, if appropriate. All are hotlinked to more detailed results further in the report. In addition, the margin of the result is indicated to provide further insight.

Figure 12. Summary report detail: The eDP software's summary report provides screen shots of all the measurements that have been performed. In this figure, you can see that many data-eye measurements were made (15 trials) and the first trial screen shot is shown. Observe the clear status and description at the top and the measurement data just above the eye.

eDP Test Point Adapters

The eDP specification is standardized on I-PEX connectors on the display panel to connect to a graphics processor board/motherboard through a ribbon-like flexible PC board.

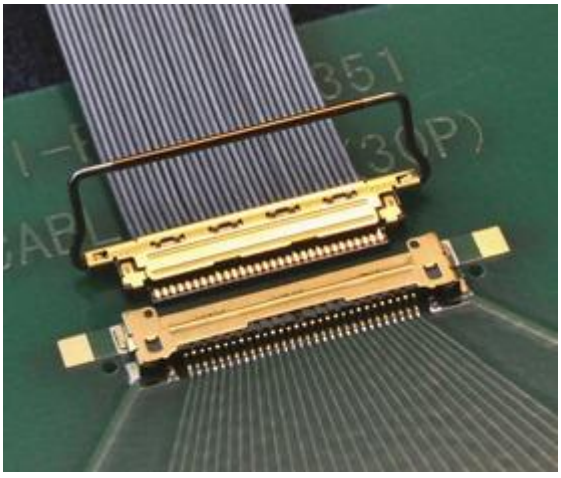


Figure 13. I-PEX connector with ribbon-like flexible PC board.

By virtue of this standardization, testing for eDP must be done at the panel connector. In DisplayPort and eDP, this point is called Testpoint 3 (or TP3 for short). TP3 necessarily includes the loss of the ribbon cable and whatever connection characteristics are at the motherboard where the ribbon connector is connected. To acquire at TP3, you will need a mating connector to your I-PEX connectorized flexible PC board. Wilder Technologies makes a family of products to connect to the flexible PC board; these are identified in the Test Accessories table below.

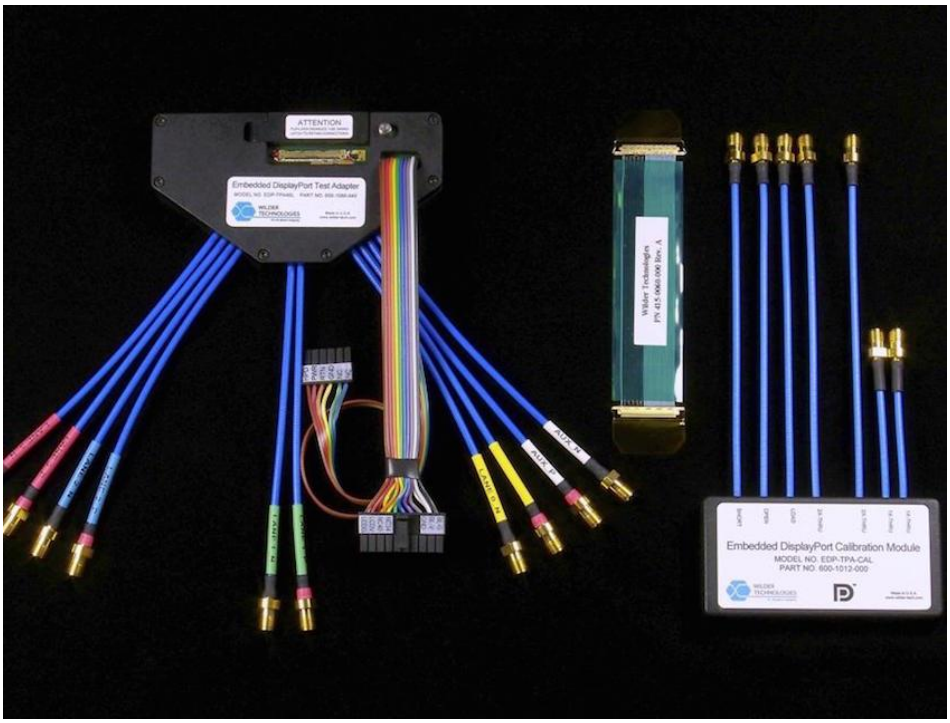


Figure 14. Wilder Technologies' eDP-TPA40L-PC test point adapter fixture.

This eDP fixture has high-speed breakout cables that terminate with SMA female connectors with an assumption that there will be cables from the oscilloscope channels to the fixture. While these cables do increase loss to the measured lines, they can be kept to a minimum to reduce their effect and can be effectively removed using PrecisionProbe software available in the Infiniium oscilloscope (see Table 4).

While TP3 will show the actual performance through a flexible PC board, it is often desired to render the acquired waveform in 'compensated' fashion to simulate a minimal correction that a receiving device might make. In DP and eDP, we call this TP3EQ (or TP3 equalized). We use CTLE (continue time linear equalizer) equalization, and the parameters for the CTLE are given in the eDP specification. The settability of these is discussed above in Device Definition.

Extensibility

You may add additional custom tests or steps to your application using the User Defined Application (UDA) development tool (www.keysight.com/find/uda). Use UDA to develop functional "Add-Ins" that you can plug into your application.

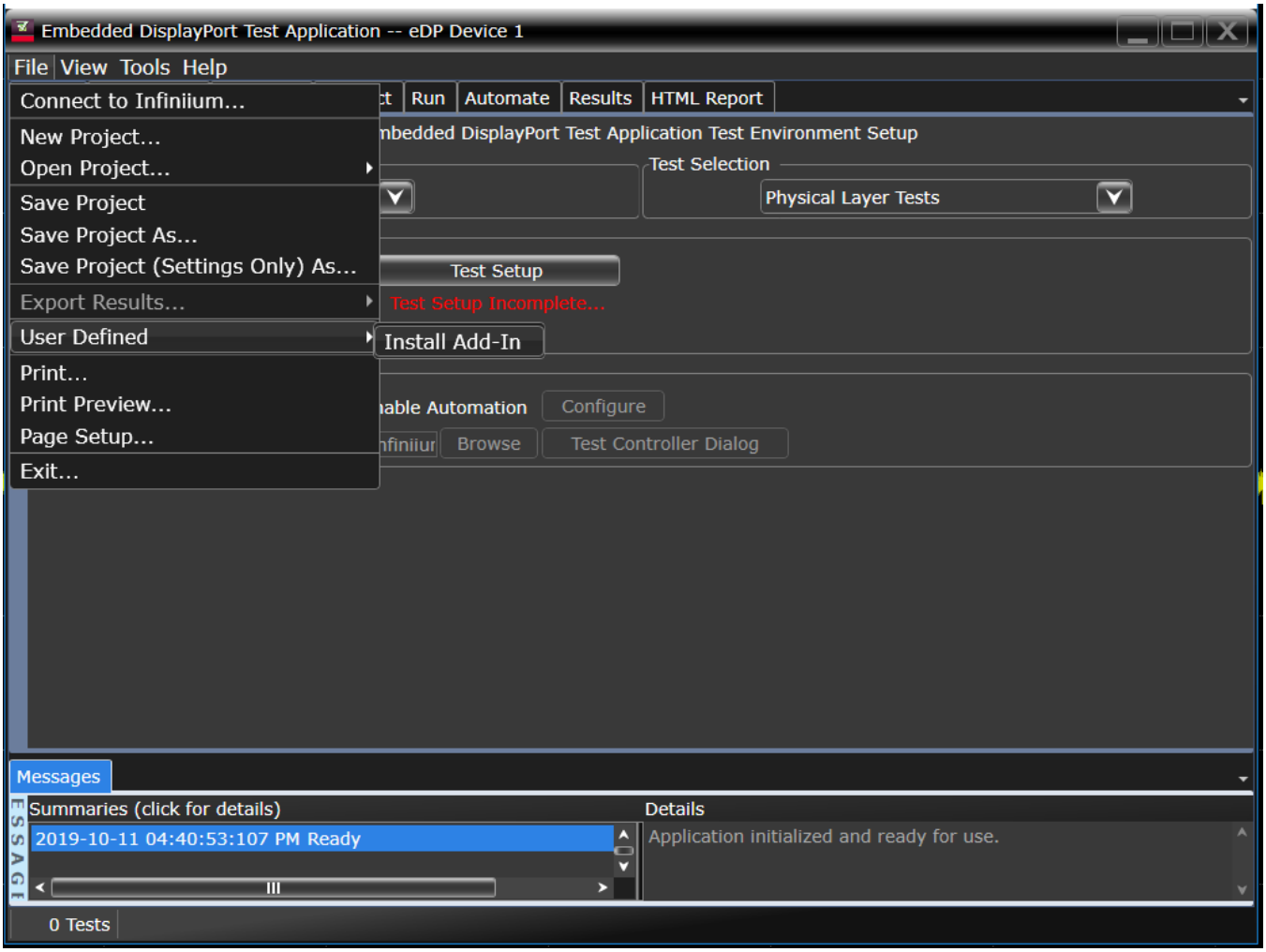


Figure 15. Importing a UDA add-in into a compliance application.

Add-ins may be designed as:

– Complete custom tests (with configuration variables and connection prompts)

– Any custom steps such as pre or post processing scripts, external instrument control and your own device control.

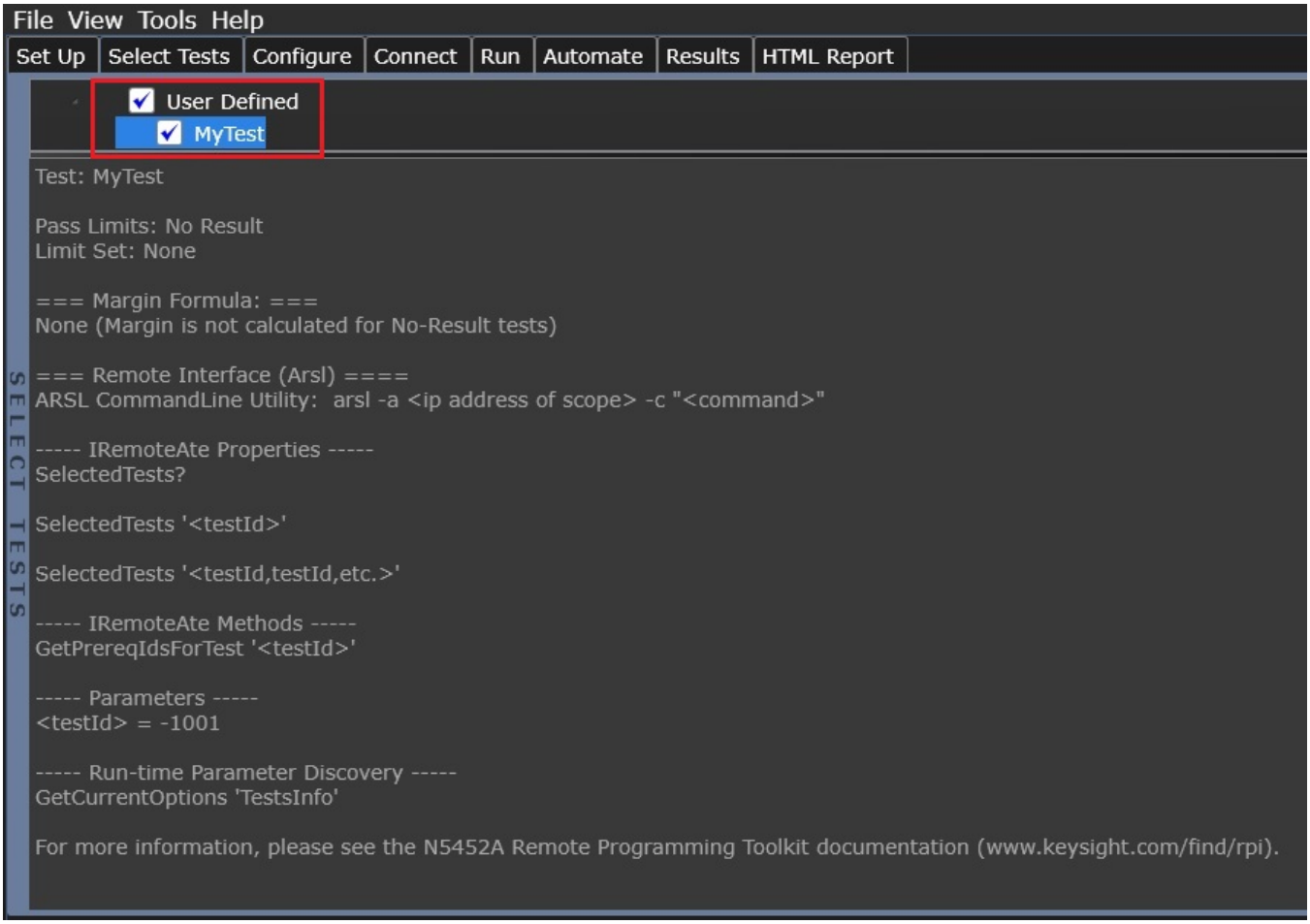


Figure 16. UDA add-in tests and utilities.

Automation

You can completely automate execution of your application's tests and Add-Ins from a separate PC using the included Remote Interface feature (download free toolkit from www.keysight. com/find/scope-apps-sw). You can even create and execute automation scripts right inside the application using a convenient built-in client.

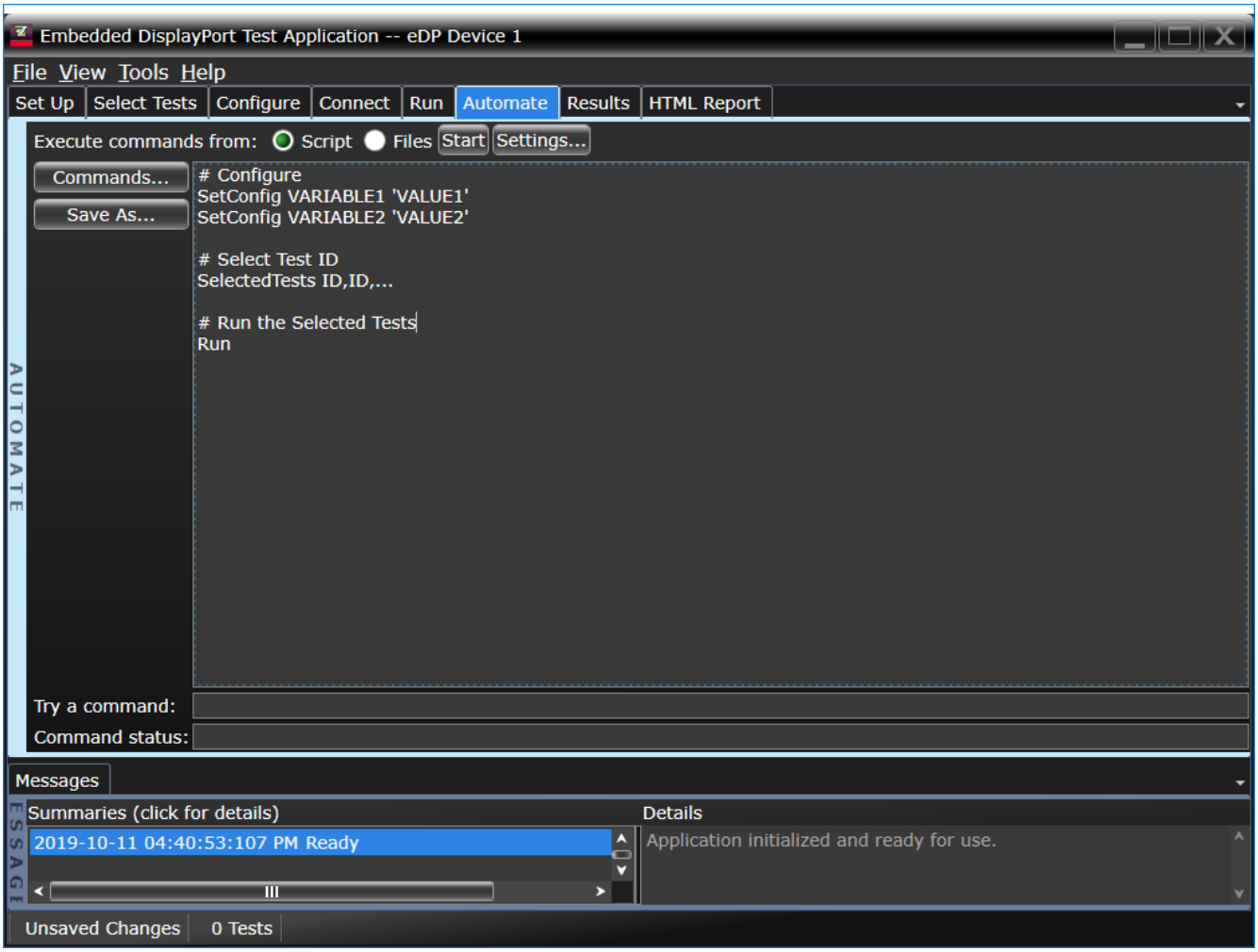


Figure 17. Remote programming script in the automation tab.

The commands required for each task may be created using a command wizard or from “Remote Interface Hint” accessible throughout the user interface.

Using automation, you can accelerate complex testing scenarios and even automate manual tasks such as:

– Opening projects, executing tests and saving results
– Executing tests repeatedly while changing configurations
– Sending commands to external instruments
– Executing tests out of order

Combine the power of built-in automation and extensibility to transform your application into a complete test suite executive:

– Interact with your device controller to place it into desired states or test modes before test execution
– Configure additional instruments used in your test suite such as a pattern generator and probe switch matrix.
– Export data generated by your tests and post-process it using your favorite environment, such as MATLAB, Python, LabVIEW, C, C++, Visual Basic etc.
– Sequence or repeat the tests and “Add-In” custom steps execution in any order for complete test coverage of the test plan.

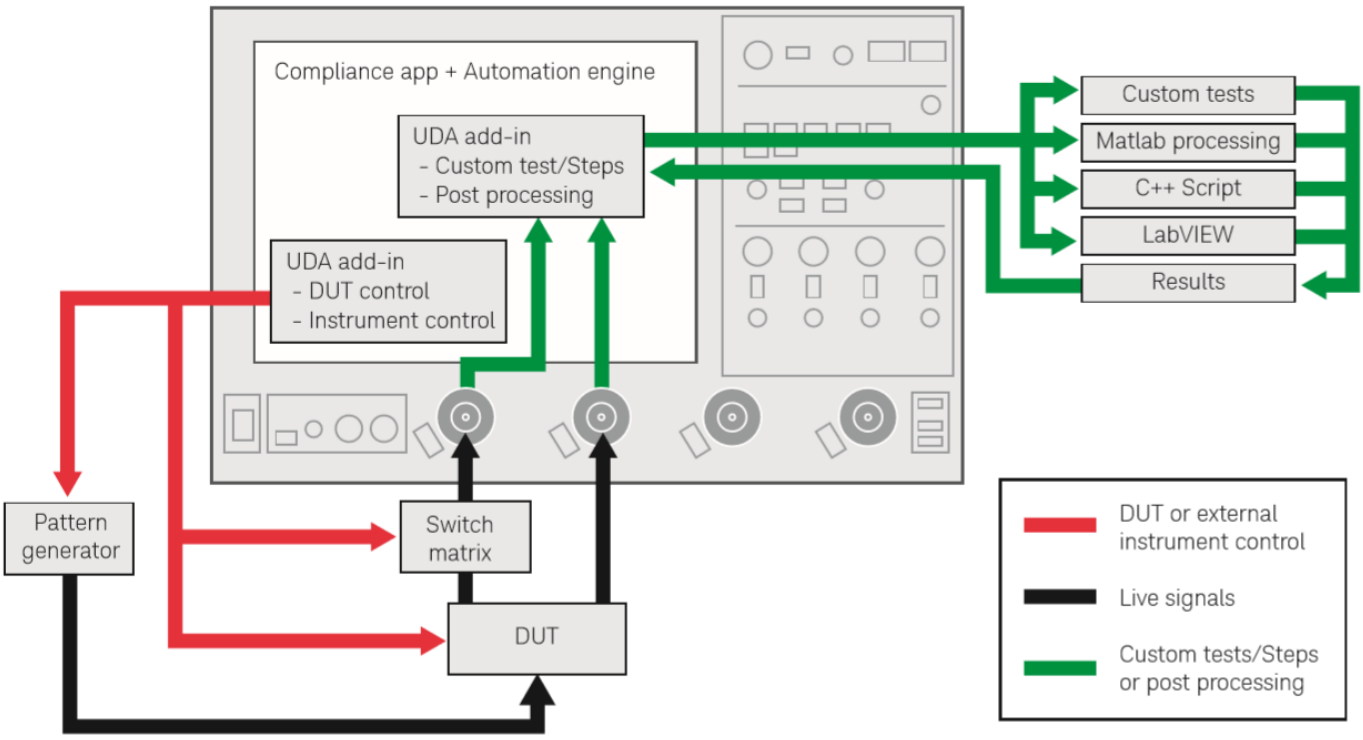


Figure 18. Combine the power of built-in automation and extensibility to transform your application into a complete test suite executive.

Tests Performed

The eDP Electrical Performance Validation software performs standard tests found in the DisplayPort electrical performance and compliance software (D9040DPPC) and are provided for the specific purpose of eDP designs. Testing is assumed to be TP3 (a flexible cable from graphics processor in place) so the user needs to consider whether TP3 or TP3Eq makes sense for their application. There is nothing that prevents a Testpoint 2 measurement except test access. If a model of the flexible cable is had (S-parameter model), a transfer function can be made to undo its effects to show what the TP2 waveform looks like.

Assertion No. *DisplayPort CTS 1.4b Section 3*	Test Description Source Tests	Test Plan	Comments
Test ID 3.1	Data eye Diagram	Yes	Custom eye mask per data rate
Test ID 3.2	Non pre-emphasis level verification	Yes	Selectable: Referential or Absolute
Test ID 3.3	Pre-emphasis level verification	Yes	Selectable:Referential or Absolute
Test ID 3.5	Intra-pair skew	Yes	D10.2 pattern required
Test ID 3.6	Differential transition time	Yes	User entry of thresholds
Test ID 3.10	AC common mode noise	Yes	Single-ended test connection required
Test ID 3.11	Non-ISI jitter measurements	Yes	Non-equalizable jitter
Test ID 3.12	Total jitter measurements	Yes	1E-9 BER
Test ID 3.14	Main link frequency compliance	Yes	D10.2 pattern preferred
Test ID 3.15	Spread spectrum modulation frequency	Yes	D10.2 pattern preferred
Test ID 3.16	Spread spectrum modulation deviation	Yes	D10.2 pattern preferred

DP tests performed by the eDP EPV software. DisplayPort CTS1.4b referenced for test definitions

Ordering Information

Recommended oscilloscope

The eDP Electrical Performance Validation software is compatible with Keysight Infiniium Series oscilloscopes with operating software revision 6.00 or higher. For oscilloscopes with earlier revisions, free upgrade software is available at www.keysight.com/find/scope-apps-sw.

Data rate	Recommended Bandwidth	Oscilloscope
Up to HBR2 (5.4 Gbs)	13GHz minimum	Infiniium V, Z and UXR series
Up to HBR3 (8.1Gbs)	16GHz recommended	Infiniium V, Z and UXR series

Note: since there is no official compliance program, the validation engineer can choose the appropriate bandwidth for system being validated.

Infiniium Measurement Software

Model number	Description	Note
D9040EDPV	Embedded DisplayPort Electrical Performance Validation Software	Required
D9020ASIA	Advanced Signal Integrity Software (EQ, InfiniiSim Advanced)	Optional
D9020JITA	Jitter, Vertical and Phase Noise Analysis Software	Optional: Recommended
D9010DMBA	Precision Cable Calibration	Optional: required if using switch matrix
D9020SCNA	InfiniiScan Event Identification Software	Optional
KS6810A	Data Analytics software (1 license)	Optional

Unattended Testing with Probes or Switch Matrix

For one connection testing with full automation in eDP either each lane is connected to a differential probe amplifier and SMA probe head, or, a switch matrix under control of the eDP Electrical Performance Validation software is used. For accuracy, direct connection to oscilloscope as always preferred, however, Keysight enables test automation through these two methods to support validation productivity.

One Connection Solution	Description	Vendor and details
Four channel Differential Connection	Amplifiers: N280xA or N700xA Probe heads: N5444A	Keysight probe solutions supported by the D9040EDPV
Switch Matrix	BIT-2100B: BIT-4000-2114-1 modules, qty=2 (4-to-1 switches) Mainframe BIT-4000-2100-1	Bitifeye Corporation, recommended integrator for Keysight solutions. Switch Matrix supported by the D9040EDPV software.

Recommended Test Accessories

For testing eDP devices, the following solution elements are recommended for the purposes identified:

Model number	Description	Quantity	Purpose
eDP-TPA30L-PC	Wilder Technologies 30 pin Test Point Adapter	1 (for 2 lane testing of eDP)	For physical connection to an Embedded DisplayPort device to perform test with the D9040eDPV software, order one or more of the these Test Point Adapters.
eDP-TPA40L-PC	Wilder Technologies 40 pin Test Point Adapter	1 (for 4 lane testing of eDP)	
N9398C	DC Blocking Capacitors	2 minimum / 4 recommended	Optionally used to eliminate dc bias in generator during test.
5061-5311	3.5mm f-f adapter	4 minimum / 8 recommended	Connect matched cables to break out coaxial connector of TPA
N2823A	1 m matched cable set	2 minimum	Optional: Connect scope to TPA break outs
N5448B	0.25 m matched cable set	2 minimum	Optional: Connect scope to TPA break outs

AUX Channel Controller

The Keysight D9040EDPV DisplayPort Electrical Performance Validation software now supports test automation with the an AUX channel controller if the DP test mode is supported by the device under test.

Model Number	Description	Quantity
Unigraf DPR-100	AUX channel controller requires hardware and software license from Unigraf Oy. www.unigraf.fi	1

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