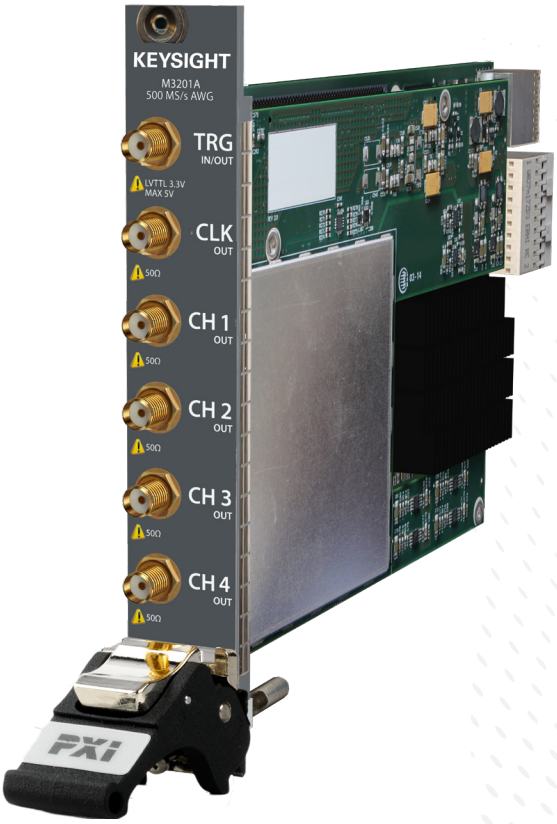
DATA SHEET

M3201A PXIe Arbitrary Waveform Generator

with Optional Real-Time Sequencing and FPGA Programming

500 MSa/s, 16 Bits, 4 Channels



KEYSIGHT TECHNOLOGIES

Generate High-Precision, Complex, Real-World Signals

The M3201A high-performance, high-bandwidth arbitrary waveform generator combines an advanced waveform generation system with embedded function generators and modulators (frequency/phase/amplitude) for broadband and IF signal generation. Performance meets simplicity thanks to easy-to-use programming libraries, real-time sequencing technology (Hard Virtual Instrumentation or HVI technology), and graphical FPGA programming technology.

Features

500 MSa/s, 16 bits, 4 channels, 200 MHz BW (400 MHz IQ)

Embedded advanced arbitrary waveform generators (AWGs)
- Advanced triggering and marking (up to 8 reconfigurable I/Os)
- Waveform queue system with cycles, delays and prescalers

Embedded high-precision function generators (FGs)
- Sinusoidal, triangular, square, DC, and more
- 45-bit frequency resolution (up to ~ 5.68 µHz)
- 24-bit phase resolution (up to ~ 21.5 µdeg)

Embedded ultra-flexible amplitude and angle modulators

High-quality output signal with low phase noise
- SFDR: 64 dBc @80 MHz (typ.)
- Average noise density: down to –145 dBm/Hz (typ.)

Optional features
- Simultaneous amplitude and angle modulations

Optional HW programming for high-performance applications
- Real-time sequencing (HVI technology)
- FPGA programming
  - Xilinx Kintex-7 325T or 410T FPGA

Up to 2 GB of onboard RAM (~ 1 Gsamples)

Mechanical/interface
- 1 slot 3U (PXIe)
- PCIe Gen 2
- Independent direct memory access (DMA) channels for fast and efficient data transfer

Applications

MIMO, beam forming and other multi-channel coherent signal generation

Manufacturing in wireless devices, automated test equipment (ATE)

General purpose, RF/arbitrary waveform generation

R&D/scientific research equipment, aerospace & defense (A/D)

Programming Technology and Software Tools

Software programming

- Easy-to-use native programming libraries for most common languages: C, C++, Visual Studio, LabVIEW, MATLAB, Python, and more

Hardware programming (optional)

- Real-time sequencing (Hard Virtual Instrumentation or HVI technology)
  - Graphical flowchart-style M3601A design environment (-HV1 option required on HW)
  - Ultra-fast, fully-parallelized, hard real-time execution
  - Ultra-fast, time-deterministic decision-making
  - Off-the-shelf inter-module synchronization & data exchange
- FPGA programming
  - Graphical M3602A FPGA design environment (-FP1 option required on HW)
  - No FPGA know-how required
  - Include from high-level to low-level design elements: off-the-shelf DSP blocks, MATLAB/Simulink designs, Xilinx CORE Generator IP cores, Xilinx VIVADO/ISE projects, VHDL or Verilog code
  - Ultra-fast, one-click compiling and on-the-fly programming

No programming

- Ready-to-use SD1 SPF (software front panels)

PXIe Arbitrary Waveform Generators, Digitizers and Combination Modules

Product	Type	Outputs (AWGs)				Inputs (Digitizers)			
		Speed (MSa/s)	Bits	Ch	BW (MHz)	Speed (MSa/s)	Bits	Ch	BW (MHz)
M3202A	AWG	1000	14	4	DC-400				
M3201A	AWG	500	16	4	DC-200				
M3102A	Digitizer					500	14	4	DC-200
M3100A	Digitizer					100	14	4/8	DC-100
M3302A	Combo	500	16	2	DC-200	500	14	2	DC-200
M3300A	Combo	500	16	2/4	DC-200	100	14	4/8	DC-100

Functional Block Diagram

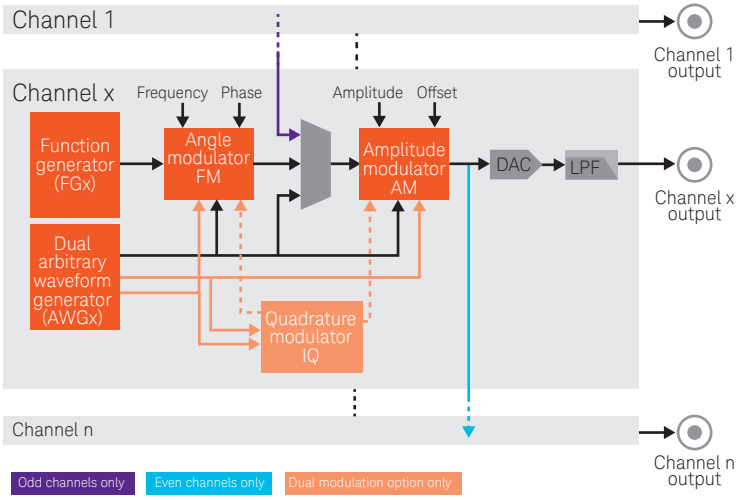


Figure 1. M3201A output functional block diagram, all channels have identical output structure

Ordering Information [1]

Product	Description
M3201A	PXI arbitrary waveform generator: 500 MSa/s, 16 Bits
Options	**Description**
M3201A-CH4	Four channels
M3201A-CLF	Fixed sampling clock, low jitter
M3201A-DM1	Dual modulation capability (amplitude and angle simultaneously)
M3201A-M01 / -M12 / -M20	Memory 16 MB, 8 MSamples / 128 MB, 60 MSamples / 2 GB, 1 GSamples
HW programming options	**Description**
M3201A-HVI	Enabled HVI programming, requires an HVI design environment license (M3601A)
M3201A-FP1	Enabled FPGA programming, requires -K32 or -K41 option and an FPGA design environment license (M3602A)
M3201A-K32 / -K41	FPGA, Xilinx 7K325T / 7K410T, required for -FP1 option only (needs memory option -M20)

Related software	Description
M3601A	HVI design environment
M3602A	FPGA design environment

1. All options must be selected at time of purchase and are not upgradable

Technical Specifications and Characteristics

General characteristics

Parameter	M3201A-CH4 Min	Typ	Max	Units	Comments
Inputs and outputs					
Channels (single-ended mode)		4		Out	
Channels (differential mode)		2		Out	Differential uses 2 channels
Reference clock [1]		1		Out	
Reference clock [2]		1		In	
Triggers/markers [1, 3]		1		In/out	Reconfigurable
Triggers/markers [2, 3]		8		In/out	Reconfigurable
Output channels overview					
Sampling rate	0.005	500	500	MSa/s	
Voltage resolution		16		Bits	
Output frequency	DC		200	MHz	
Real-time BW			200	MHz	
Output voltage	–1.5		1.5	Volts	
Built-in functionality					
Function generators		4			1 per channel
Dual AWGs		4			1 per channel
IQ modulators		4			1 per channel
Frequency modulators		4			1 per channel
Phase modulators		4			1 per channel
Amplitude modulators		4			1 per channel
DC offset modulators		4			1 per channel
Onboard memory					
RAM memory	16		2048	MBytes	

1. At front panel
2. At backplane
3. Markers available from firmware version v3.0 or later

I/O specifications

Parameter	M3201A-CH4 Min	Typ	Max	Units	Comments
Output channels					
Sampling rate [1]	0.005		500	MSa/s	
Output frequency	DC		200	MHz	Limited by a reconstruction filter
Output voltage	–1.5		1.5	Volts	On a 50 Ω load
Source impedance		50		Ω	
Reference clock output					
Frequency		10 or 100		MHz	Generated from the internal clock, user selectable
Voltage		800		mV_{pp}	On a 50 Ω load
Power		2		dBm	On a 50 Ω load
Source impedance		50		Ω	AC coupled
External I/O trigger/marker					
V_{IH}	2		5	V	
V_{IL}	0		0.8	V	
V_{OH}	2.4		3.3	V	On a high Z load
V_{OL}	0		0.5	V	On a high Z load
Input impedance		10		K Ω	
Source impedance		TTL		–	
Speed		100		MHz	

1. (-CLF) option: fixed 500 MSa/s

Function generators (FGs) specifications

Parameter	M3201A-CH4 Min	Typ	Max	Units	Comments
General specifications					
Function generators		4		–	1 per channel
Waveform types		4		–	Sinusoidal, triangular, square and DC
Frequency range	0		200	MHz	
Frequency resolution		45		Bits	
Frequency resolution		5.7		µHz	
Phase range	0		360	Deg	
Phase resolution		24		Bits	
Phase resolution		21.5		µdeg	
Speed performance					
Frequency change rate		100		MChanges/s	With HVI technology
Frequency modulation rate		500		MSamples/s	With AWGs and angle modulators
Phase change rate		100		MChanges/s	With HVI technology
Phase modulation rate		500		MSamples/s	With AWGs and angle modulators

Amplitude and offset specifications

Parameter	M3201A-CH4 Min	Typ	Max	Units	Comments
General specifications					
Amplitude / offset range	–1.5		1.5	Volts	Amplitude + offset values
Amplitude / offset resolution		16		Bits	
Amplitude / offset resolution		45.8		µV	
Speed performance					
Amplitude / offset change rate		500		MChanges/s	With HVI technology
Amplitude / offset modulation rate		500		MSamples/s	With AWGs and amplitude modulators

Arbitrary waveform generators (AWGs) specifications

Parameter	M3201A-CH4 Min	Typ	Max	Units	Comments
General specifications					
Dual AWGs		4			1 dual AWG per output channel
Aggregated speed (16 bits)			4000	MSa/s	For all onboard waveforms combined
Aggregated speed (32 bits)			2000	MSa/s	For all onboard waveforms combined
Waveform multiple		5		Samples	Waveform length must be a multiple of this value
16-bit waveform length	15		957M	Samples	Maximum depends on onboard RAM
32-bit waveform length	10		478M	Samples	Maximum depends on onboard RAM
Waveform length efficiency		93.5		%	Effic. = waveform size / waveform size in RAM
Trigger		Selec.			External trigger (input connector, backplane triggers), software trigger
AWG specifications (16-bit single waveform)					
Speed			500	MSa/s	Per AWG
Resolution		16		Bits	
AWG destination		Selec.			Amplitude, offset, frequency or phase
AWG specifications (16-bit dual waveform)					
Speed (waveform A)			500	MSa/s	Per AWG
Speed (waveform B)			500	MSa/s	Per AWG
Resolution (waveform A)		16		Bits	
Resolution (waveform B)		16		Bits	
AWG destination (waveform A)		Selec.			Amplitude, offset or I
AWG destination (waveform B)		Selec.			Frequency, phase or Q
AWG specifications (32-bit single waveform)					
Speed			100	MSa/s	Per AWG, minimum prescaler: 1
Resolution		32		Bits	
AWG destination		Selec.			Amplitude, offset, frequency or phase
AWG specifications (32-bit dual waveform)					
Speed (waveform A)			100	MSa/s	Per AWG, minimum prescaler: 1
Speed (waveform B)			100	MSa/s	Per AWG, minimum prescaler: 1
Resolution (waveform A)		32		Bits	
Resolution (waveform B)		32		Bits	
AWG destination (waveform A)		Selec.			Amplitude or offset
AWG destination (waveform B)		Selec.			Frequency or phase

Angle modulators specifications

Parameter	M3201A-CH4 Min	Typ	Max	Units	Comments
General specifications					
Frequency modulators		4			1 per output channel
Phase modulators		4			1 per output channel
Carrier signal source		FGs			Table 3 on page 7
Modulating signal source		AWGs			Table 5 on page 8
Frequency modulators (16-bit modulating waveform)					
Deviation	–Dev. gain		+Dev. gain	MHz	
Modulating signal resolution		16		Bits	AWG waveform
Modulating signal BW	0		250	MHz	AWG Nyquist limit
Deviation gain	0		200	MHz	
Deviation gain resolution		16		Bits	
Frequency modulators (32-bit modulating waveform)					
Deviation	–Dev. gain		+Dev. gain	MHz	
Modulating signal resolution		32		Bits	AWG waveform
Modulating signal BW	0		50	MHz	AWG Nyquist limit
Deviation gain	0		200	MHz	
Deviation gain resolution		16		Bits	
Phase modulators (16-bit modulating waveform)					
Deviation	–Dev. gain		+Dev. gain	Deg	
Modulating signal resolution		16		Bits	AWG waveform
Modulating signal BW	0		250	MHz	AWG Nyquist limit
Deviation gain	0		180	Deg	
Deviation gain resolution		16		Bits	~ 5.5 mdeg
Phase modulators (32-bit modulating waveform)					
Deviation	–Dev. gain		+Dev. gain	Deg	
Modulating signal resolution		16		Bits	AWG waveform is truncated
Modulating signal BW	0		50	MHz	AWG Nyquist limit
Deviation gain	0		180	Deg	
Deviation gain resolution		16		Bits	~ 5.5 mdeg

Amplitude modulators specifications

Parameter	M3201A-CH4 Min	Typ	Max	Units	Comments
General specifications					
Amplitude modulators		4			1 per output channel
Offset modulators		4			1 per output channel
Carrier signal source		FGs			Table 3 on page 7
Modulating signal source		AWGs			Table 5 on page 8
Amplitude & offset modulators (16-bit modulating waveform)					
Deviation	–Dev. gain		+Dev. gain	V_p	
Modulating signal resolution		16		Bits	AWG waveform
Modulating signal BW	0		250	MHz	AWG Nyquist limit
Deviation gain	0		1.5	V_p	
Deviation gain resolution		16		Bits	Limited by the output DAC
Amplitude & offset modulators (32-bit modulating waveform)					
Deviation	–Dev. gain		+Dev. gain	V_p	
Modulating signal resolution		16		Bits	AWG waveform is truncated
Modulating signal BW	0		50	MHz	AWG Nyquist limit
Deviation gain	0		1.5	V_p	
Deviation gain resolution		16		Bits	Limited by the output DAC

IQ modulators specifications

Parameter	M3201A-CH4 Min	Typ	Max	Units	Comments
General specifications					
IQ modulators		4			1 per output channel
Carrier signal source		FGs			Table 3 on page 7
Modulating signal source		AWGs			Table 5 on page 8
Amplitude deviation	–1.5		–1.5	V_p	
Phase deviation	–180		180	Deg	
I modulating signal resolution		16		Bits	AWG waveform
I modulating signal BW	0		250	MHz	AWG Nyquist limit
Q modulating signal resolution		16		Bits	AWG waveform
Q modulating signal BW	0		250	MHz	AWG Nyquist limit

Clock system specifications

Parameter	M3201A-CH4 Min	Typ	Max	Units	Comments
General specifications					
Clock frequency[1]	>100		500	MHz	

1. (-CLF) option: fixed 500 MSa/s

AC performance

Parameter	M3201A-CH4 Min	Typ	Max	Units	Comments
General characteristics					
Analog output jitter		<2		ps	RMS (cycle-to-cycle)
AWG trigger to output jitter		<2		ps	RMS (cycle-to-cycle) for any trigger referenced to the chassis clock; independent of input trigger jitter if input jitter < 4nS peak-to-peak
Trigger resolution		10		ns	
Channel-to-channel skew		<20		ps	Between ch 0 & ch 1, and ch 2 & ch 3
		<50		ps	Between any channel
		<150		ps	Between modules, chassis dependent [2]
Clock output jitter		<2		ps	RMS (cycle-to-cycle)
Clock accuracy and stability		100		ppm	PXIe, cPXIe versions; chassis dependent[1]
AC characteristics					
Spurious-free dynamic range (SFDR)					P_{out} = 0 dBm, measured from DC to max frequency
f_{out} = 10 MHz		68		dBc	
f_{out} = 80 MHz		64		dBc	
f_{out} = 120 MHz		57		dBc	
f_{out} = 160 MHz		54		dBc	
Crosstalk (adjacent channels)					
f_{out} = 10 MHz		<–105		dB	
f_{out} = 80 MHz		–75		dB	
f_{out} = 120 MHz		–88		dB	
f_{out} = 160 MHz		–73		dB	
Crosstalk (non-adjacent channels)					
f_{out} = 10 MHz		<–105		dB	
f_{out} = 80 MHz		–78		dB	
f_{out} = 120 MHz		<–105		dB	
f_{out} = 160 MHz		–92		dB	
Phase noise (SSB)					
offset = 1 kHz		<–127		dBc/Hz	
offset = 10 kHz		<–133		dBc/Hz	
offset = 100 kHz		<–138		dBc/Hz	
Average noise power density		<–145		dBm/Hz	

1. This value corresponds to a chassis that fulfils the PXI Express specifications. This value can be improved with an external chassis clock or a System Timing Module.
2. This value corresponds to a M9005A PXIe chassis.

AC performance, typical

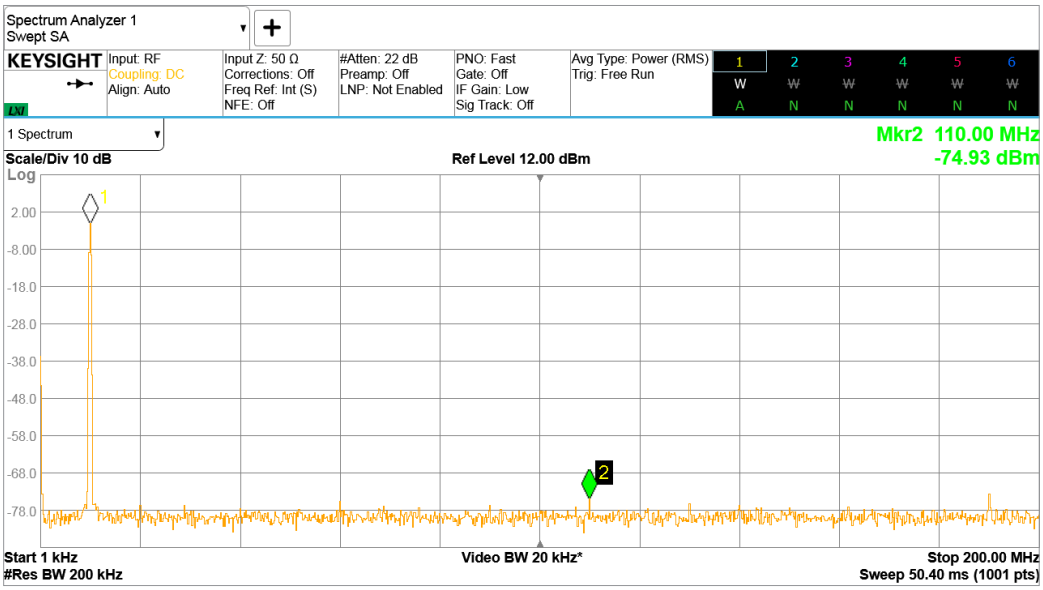


Figure 2. Single-tone spectrum @ f_{out} = 10 MHz

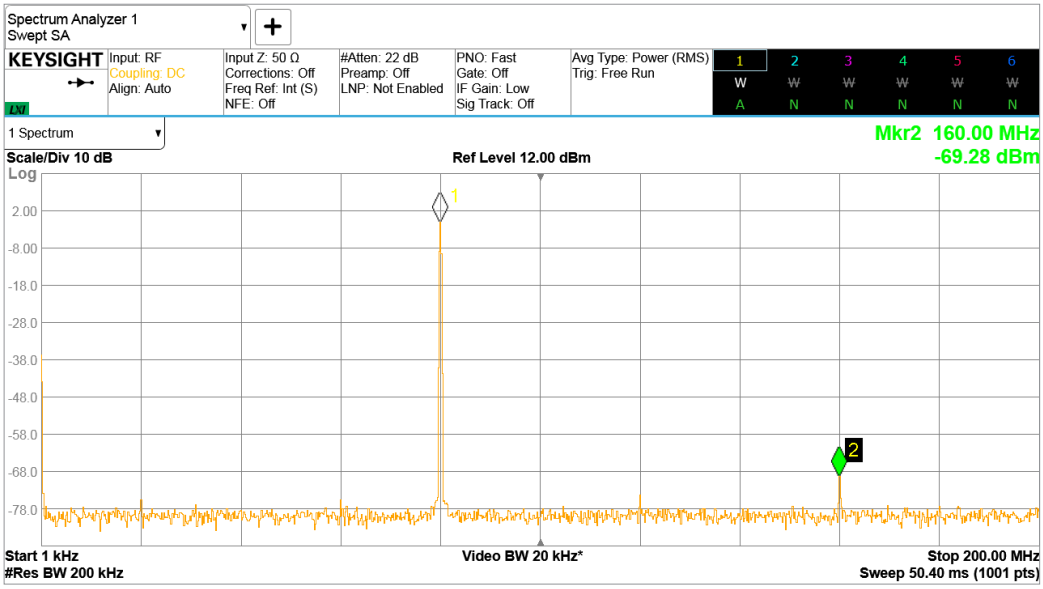


Figure 3. Single-tone spectrum @ f_{out} = 80 MHz

AC performance, typical

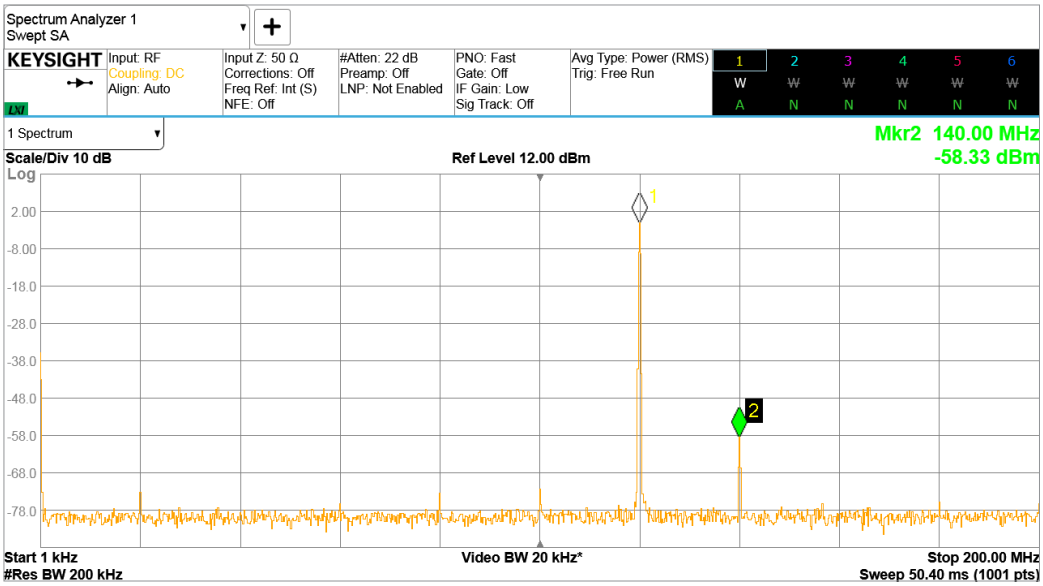


Figure 4. Single-tone spectrum @ f_{out} = 120 MHz

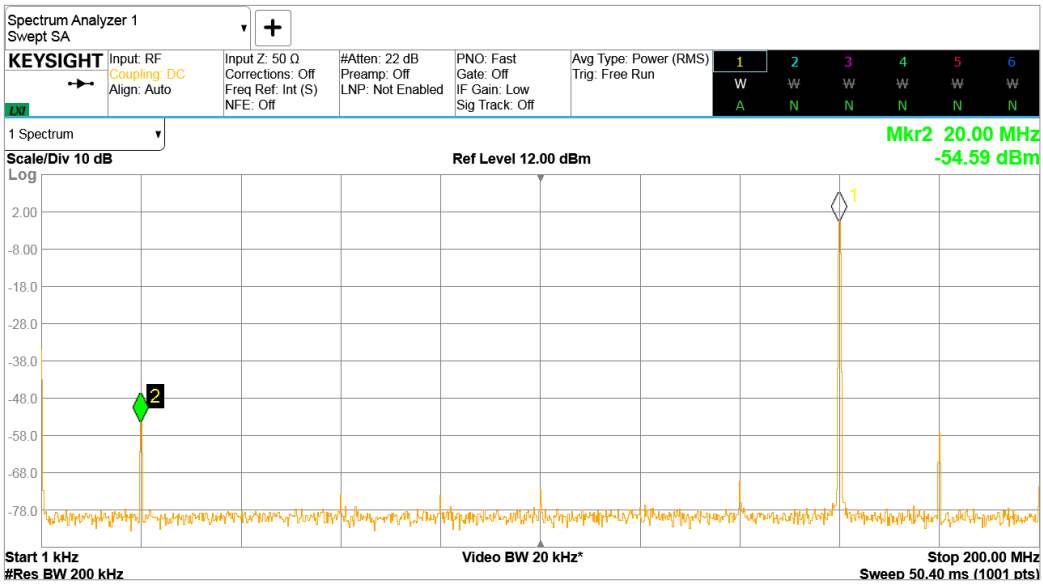


Figure 5. Single-tone spectrum @ f_{out} = 160 MHz

System Specifications

Environmental specifications (PXI Express)

Parameter	M3201A-CH4 Min	Typ	Max	Units	Comments
System bus					
Slots		1		Slot	PXI Express (CompactPCI Express compatible)
PCI Express type	Gen 1		Gen 2	–	Automatic gen negotiation, chassis dependent
PCI Express link	1		4	Lanes	Automatic lane negotiation, chassis dependent
PCI Express speed	400		1600	MBytes/s	Depends on # of lanes, chassis, congestion, and more
Power and temperature					
3.3 V PXIe power supply		1.5		A	~ 5 W
12 V PXIe power supply		2		A	~ 24 W

Environmental [1]		
Temperature range	Operating Non-operating	0 to +55°C (10,000 feet) -40 to +70 °C (up to 15,000 feet)
Max operative altitude		4000 m (10,000 feet)
Operating Humidity range (%RH)		10 to 95% at 40 °C
Non-operating Humidity range (%RH): 5 to 95		5 to 95%
Calibration interval		1 year
EMC		Complies with European EMC Directive – IEC/EN 61326-1 – CISPR Pub 11 Group 1, class A This ISM device is in compliance with Canadian ICES-001 Cet appareil ISM est conforme à la norme NMB-001 du Canada. This ISM device is in compliance with Australian and New Zealand RCM This ISM device is in compliance with South Korea EMC KCC

1. Samples of this product have been type tested in accordance with the Keysight Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation and End-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude and power line conditions. Test Methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3.

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