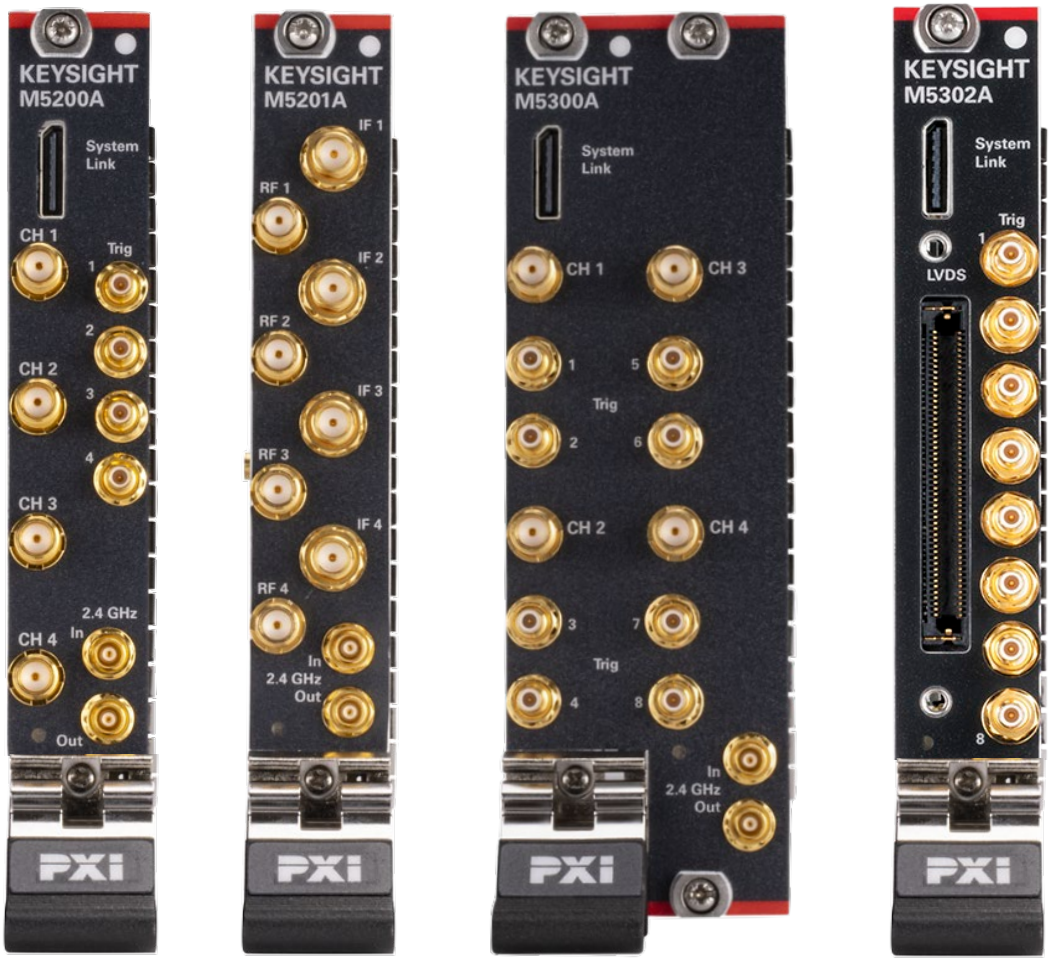
M5000 Series

High-Performance PXI System



KEYSIGHT

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Meet the M5000 Series

Welcome to the all-new Keysight M5000 Series. With an RF AWG, digitizer, digital I/O, and downconverter modules, the M5000 Series is a high-performance PXI system that enables the latest innovations in quantum, aerospace defense, and more.

M5000 Series product overview [1]

Model	Description
M5200A	PXIe Digitizer 4 Channels, 2 GHz BW, 12-bit
M5201A	PXIe Down Converter 4 Channels, 2-16 GHz RF, 0.01-2.4 GHz IF
M5300A	PXIe RF AWG 4 Channels, DC-16 GHz RF, 2 GHz IBW, 14-bit
M5302A	PXIe Digital I/O 28 LVDS Channels, 8 Trigger Channels

Related products

Model	Description
M9046A	PXIe Chassis: High power, 18 slots, 24 GB/s, Requires option -QS2
M9032A	PXIe System Synchronization Module, 2-port
M9033A	PXIe System Synchronization Module, 5-port
M9037A	PXIe Embedded Controller
M9614A	PXIe 5-channel Source/Measure Unit
M9615A	PXIe 5-channel Precision Source/Measure Unit
P5000B	Streamline Vector Network Analyzer
UXR0164A	Infiniium UXR-Series Oscilloscope: 16 GHz, 4 Channels

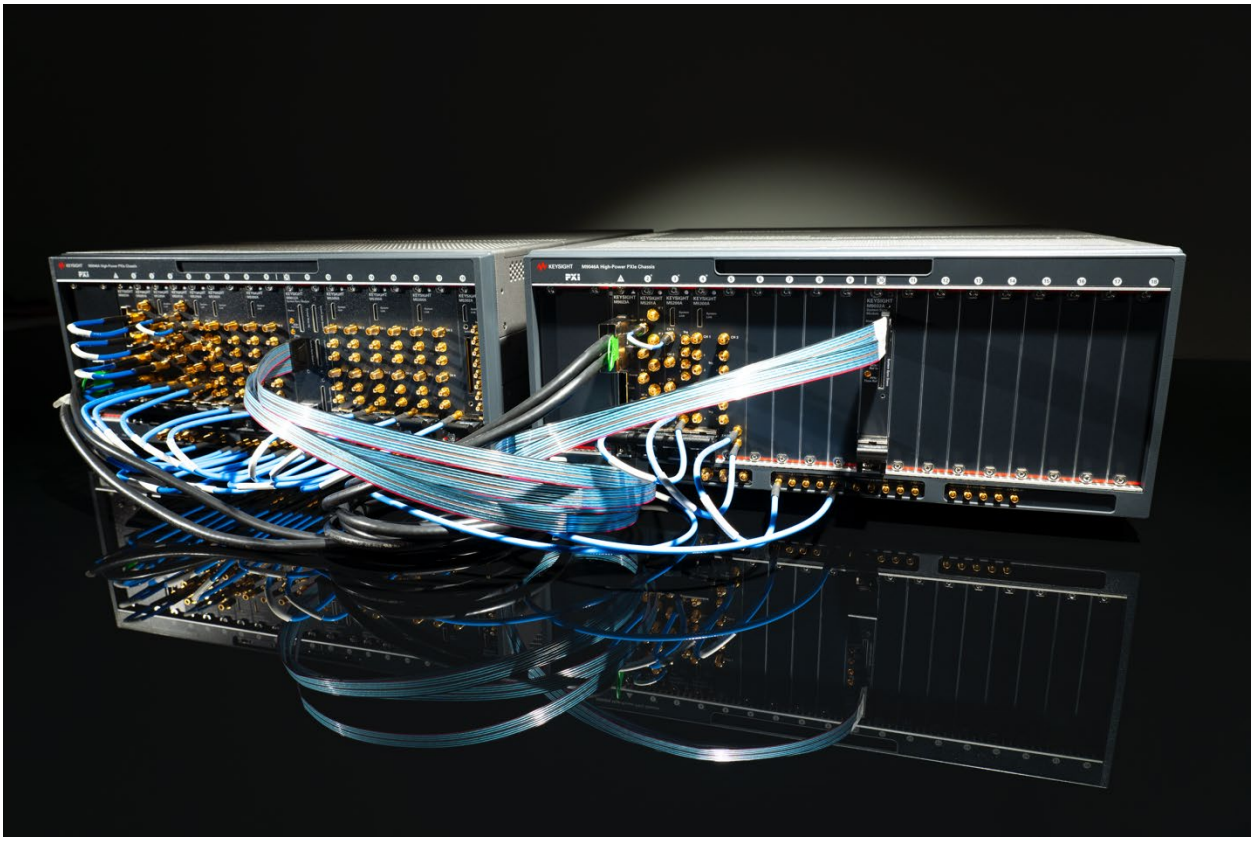
[1] See data sheet spec tables to learn more.

Enabling the Latest Innovations

Quantum control

The M5000 Series forms the backbone for the Keysight Quantum Control System (QCS) – complete digital solution that eliminates the need to design custom control solutions.

Analog LOs and mixers in traditional hardware used for quantum control require frequent calibration, introduce leakage noise, and contribute to slow drifts in the performance of the system. The Keysight M5000 Series fully eliminates the need for these components leading to enhanced ease-of-use, unrivaled noise performance, and improved long-term stability.



M5000 Series Modules

M5200A Digitizer

The M5200A is a single-slot PXIe four-channel, high-speed digitizer. It is a high-performance digitizer with easy-to-use programming libraries, real-time sequencing technology, and FPGA programming.

The digitizer module supports four 2 GHz channels with 4.8 GSa/s sampling rate and 12-bits of resolution for high-definition sampling in quantum computing and aerospace applications. Users can create IP and processing algorithms in the FPGA. Users also have the ability for data usage outside of the module with the ability to stream data directly over the PCIe backplane.

M5201A Downconverter

The M5201A is a single-slot PXIe low-IF downconverter module with four pairs of RF/IF channels and a single, shared, internal local oscillator (LO). The RF input frequency range is 2 to 16 GHz. The intermediate frequency (IF) ranges from 10 MHz to 2.4 GHz.

The clock generator on the M5201A provides a reference which is then used to generate the Local Oscillator (LO) frequency required for the application. Inputs to the clock generator include the front panel 2.4 GHz clock input, the 100 MHz PXIe clock, and DSTAR clock from the chassis. When used with the -QS1 option on the M9046A chassis, the 2.4 GHz clock provides minimal phase noise and drift.

M5300A RF AWG

The M5300A is a two-slot PXIe module with four high-speed AWG outputs, clock input and output, and eight triggers. It provides high-performance with easy-to-use programming libraries, real-time sequencing technology, and FPGA programming.

The M5300A RF AWG module supports four directly synthesized RF channels in 2 PXIe slots with up to 16 GHz of RF and 2 GHz of instantaneous bandwidth using direct digital I/Q modulation. The M5300A provides a waveform memory per channel of 1 GSample – half real (I) samples and half imaginary (Q) samples.

The M5300A includes a PathWave FPGA with user-customizable customer accessible area. The FPGA resource reserved for the customer configurable area is approximately 25% of the total XVCU35P FPGA resources. The customer configurable area in the M5300A reserves approximately 98% of CLB registers and 98% of LUTs for the user application.

M5302A Digital I/O

The M5302A is a single-slot Digital I/O PXIe module with 28 programmable LVDS channels and 8 single-ended channels. The LVDS channels can be used to communicate to the device under test or can be used to control other devices by emulating protocols. The single-ended channels are suitable for event triggers or other general-purpose I/O applications.

There are 28 bidirectional differential channels included on a 100-pin, front panel connector. These differential signals are LVDS (meant to drive 100-ohm differential load) and have a 1.2 Gbps maximum toggle rate. The Dig connector also includes +5 V power that is available to the user to power external interface circuitry (maximum current load is 0.5 A).

Eight SMBs are available for instrument triggers or other general purpose I/O signals. These channels are single-ended with a voltage swing of 0 – 3.3 V when driving High Impedance loads (the voltage levels at the DUT are halved when connected to a 50 Ω load). These signals can toggle up to 150 MHz when used as outputs, and 75 MHz when used as inputs.

Distributed processing with FPGA

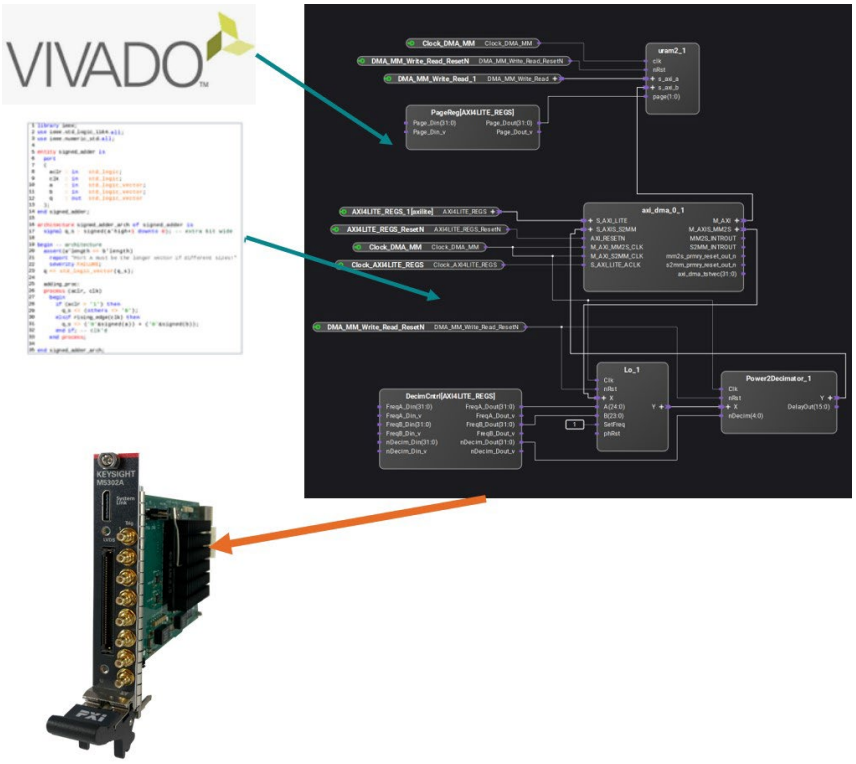
The M5000 Series has individual FPGAs in each module. Featuring the Kintex UltraScale+ FPGA in the M5201A and M5302A, and the Virtex UltraScale+ FPGA in the M5200A, M5300A, and M5301A, which allow for fast, distributed processing. The FPGA configurable region utilizes Xilinx FPGA partial reconfiguration technology to design and configure a defined section of the FPGA without the need to power down or reboot the cards or host computer.

PathWave FPGA

PathWave FPGA is a graphical environment that provides the ability to rapidly develop FPGA designs on many Keysight instruments. An IP library includes Logic/Math, Memory and DSP blocks that can be included in an FPGA design. PathWave FPGA supplies components to create custom design flows to go quickly from schematic to bitfile generation with the press of a button.

PathWave FPGA ships with a rich set of built-in library elements that can be dropped into a schematic. Easily modify the default template by importing Vivado IP, HDL IP, or by using the PathWave FPGA IP library. Key benefits:

- Visualize application flows and insert custom blocks
- Streamline the design process with full native FPGA-code compatibility
- Quickly compile the bitfile to program the FPGA model embedded in the instrument
- Easily target different instrument FPGAs using Board Support Packages (BSPs)

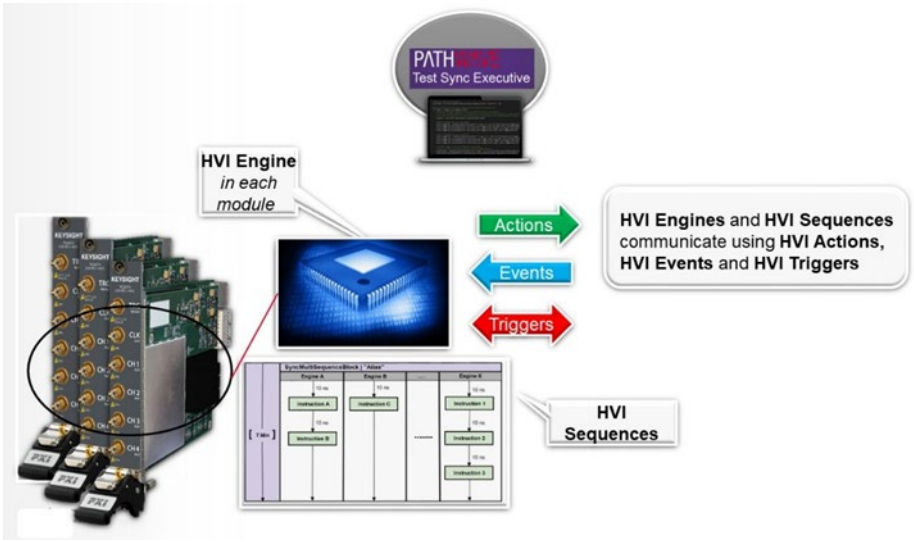


PathWave Test Sync Executive

PathWave Test Sync Executive enables rapid development of high performance, multi-channel and multi-instrument, real-time synchronous solutions. This powerful software tool is critical in applications requiring tight synchronization, control, and feedback, including quantum control, radar, communication systems, and more.

With seamless integration of PathWave FPGA supported by the M5000 Series modules, you can now achieve:

- Transparent multi-module synchronization by precisely time aligning multiple channels in the same module or across several modules
- Real-time synchronous execution including sequencing, branching, and looping
- Time-deterministic hardware-based execution



Technical Specifications and Characteristics

M5200A characteristics

General characteristics	
Description	PXIe high-speed digitizer
Bus interface and compatibility	PXIe peripheral module (x8 Gen 3)
Number of slots	1
PXIe chassis compatibility	M9046A
Front panel connectors	
RF Input connectors	SMA (4)
Trigger I/O	SMB (4)
2.4 GHz in	MCX
2.4 GHz out	MCX
Mechanical (nom)	
Size	3U/1-slot PXIe standard 130.1 x 21.7 x 210 mm; includes connectors and handle extensions
Weight	419 g (0.9 lb)

Digitizer characteristics	
Sampling rate	4.8 GSa/s
Resolution	12-bit
Input impedance (warranted)	50 Ohm, ± 1 Ohm
DC gain accuracy (warranted)	± 2%
DC offset accuracy (warranted)	± 1.5%
3 dB bandwidth (warranted)	≥ 2 GHz
Coupling	DC
Bandwidth	DC-2 GHz
Input voltage full-scale range	900 mV pk-pk (module default gain setting)
RMS noise (at nominal full-scale range)	< 800 uV
Effective Number of Bits (ENOB)	8
Memory Depth	1 GSa/Ch
Spurious free dynamic range (SFDR) (50% Full-Scale)	65 dBc
Spurious free dynamic range (SFDR) (80% Full-Scale)	65 dBc up to 1 GHz 40 dBc up to 2 GHz

Clock and I/O characteristics

Module reference clock		
Clock sources	Front panel, PXI_CLK100	
Front panel clock frequency	2.4 GHz	
Nominal input clock power	+15 dBm	
Module self-clocking	Yes	
Accuracy	Chassis dependent	
Input/output triggers		
Trigger sources	Software, PXI_TRIG, PXI_STAR, and front panel I/O	
Trigger destinations	PXI_TRIG and front panel I/O	
Trigger polarity	Active high or active low (programmable)	
Trigger jitter	100 ns	
Max PXI trigger toggle rate	100 MHz	

Trigger channel characteristics

Number of channels	4	
Channel type	Single-ended, bidirectional, ground reference	
Default state	1 MΩ nominal, input	
Output characteristics (typical)		
Ouput voltage 50 Ω load High impedance load	 0 V - 1.6 V 0 V - 3.2 V	
Maximum output channel toggle rate	150 MHz	
Input characteristics (typical)		
Input voltage range	0 - 5 V	
Maximum low voltage threshold	0.8 V	
Maximum high voltage threshold	2 V	
Load impedance	1 MΩ	
Maximum input channel toggle rate	75 MHz	

Module power requirements

Total power dissipation	45 W [2]	
Supply voltage	+3.3 V	+12 V
Supply current	5.8 A	2.2 A

FPGA characteristics

FPGA type	Xilinx Virtex Ultrascale+ (XCVU35P)
FPGA sandbox size	1/4 of FPGA resources
Timebase frequency	300 MHz (phase-locked to 100 MHz chassis clock)
Timebase source	PXI_CLK100 or DSTARA

[2] Nominal power without application specific gateware

FPGA resource estimates

Site type	Available	Used	% Utilized	Available to user
CLB LUTs	244936	9424	3.85	235512
LUT as logic	244936	9369	3.83	235567
LUT as memory	113192	55	0.05	113137
CLB registers	489872	10028	2.05	479844
Register as flip flop	489872	10028	2.05	479844
Register as latch	489872	0	0	489872
CARRY8	30617	162	0.53	30455
F7 Muxes	122468	242	0.20	122226
F8 Muxes	61234	119	0.19	61115
F9 Muxes	30617	0	0	30617
CLB	30617	3647	11.91	26970
CLBL	16468	1971	11.97	14497
CLBM	14149	1676	11.85	12473
Unique control sets	61234	1144	1.87	60090
Block RAM tile	360	0.5	0.14	359.5
RAMB36/FIFO	360	0	0	360
RAMB18	720	1	0.14	719
URAM	240	0	0	240
DSPs	1872	0	0	1872

M5201A characteristics

General characteristics

Description	PXIe down converter
Bus interface and compatibility	PXIe peripheral module (x8 Gen 3)
Number of slots	1
PXIe chassis compatibility	M9046A
LO source	Internal
Front panel connectors	
RF in	SMA (4)
IF out	SMA (4)
2.4 GHz in	MCX
2.4 GHz out	MCX
Mechanical (nom)	
Size	3U/1-slot PXIe standard 130.1 x 21.7 x 210 mm; includes connectors and handle extensions
Weight	387 g (0.85 lb)

Channel characteristics

RF in characteristics	
Frequency range	2 GHz to 16 GHz
Max input power	0 dBm
Input power damage level	+10 dBm
Port match	S11 < -10 dB up to 10 GHz S11 < -5 dB up to 16 GHz
IF out characteristics	
Channel bandwidth	10 MHz - 2400 MHz
Port match	< -10 dB
Performance characteristics	
Conversion gain (warranted) 2 GHz 14 GHz	 >0 dB
Conversion gain (typical) 2 GHz (high-side mixing) 4 GHz 10 GHz 14 GHz 16 GHz 18 GHz (low-side mixing)	 +2 dB +5 dB +3 dB +1 dB 0 dB 0 dB
LO frequency range	1 GHz to 18 GHz
LO Frequency resolution	5 x 10^{-6} Hz
LO Phase resolution	84 x 10^{-9} degrees
Input referred noise	-166 dBm/Hz
Noise figure	8 dB
Phase noise	-130 dBc/Hz at 12 GHz, 10 kHz offset
Channel to channel isolation	> 60 dB

Module power requirements

Total power dissipation	32 W [3]	
Supply voltage	+3.3 V	+12 V
Supply current	3.6 A	1.7 A

Clock and I/O characteristics

Module reference clock	
Clock sources	Front panel, PXI_CLK100
Front panel clock frequency	2.4 GHz
Nominal input clock power	+15 dBm
Module self-clocking	Yes
Accuracy	Chassis dependent
Input/output triggers	
Trigger sources	Software, PXI_TRIG, and PXI_STAR
Trigger destinations	PXI_TRIG and front panel I/O
Trigger polarity	Positive and negative support
Trigger jitter	100 ns
Max PXI trigger toggle rate	100 MHz

FPGA characteristics

FPGA type	Xilinx Kintext Ultrascale+ (KU15P)
FPGA sandbox size	1/6 of FPGA resources
Timebase frequency	300 MHz (phase-locked to 100 MHz chassis clock)
Timebase source	PXI_CLK100 or DSTARA

[3] Nominal power without application specific gateware

M5300A characteristics

General characteristics

Description	PXIe RF AWG
Bus interface and compatibility	PXIe peripheral module (x8 Gen 3)
Number of slots	2
PXIe chassis compatibility	M9046A
Front panel connectors	
Trigger channels	SMB (8)
RF connector	SMA
2.4 GHz in	MCX
2.4 GHz out	MCX
Mechanical (nom)	
Size	3U/1-slot PXIe standard 130.1 x 21.7 x 210 mm; includes connectors and handle extensions
Weight	649 g (1.4 lb)

Channel characteristics

RF characteristics	
Frequency range (warranted)	-3 dB at 15 GHz
Frequency range (typical)	-3 dB at 16 GHz -5 dB at 17 GHz -6 dB at 18 GHz
Port match	S22 < -10 dB to 10 GHz S22 < -5 dB to 16 GHz
Performance characteristics	
Baseband/Information bandwidth	2 GHz
DAC resolution	14-bit
Baseband sample rate, per-channel	4.8 GSa/s (2.4 GSa/s I/Q)
Waveform memory depth, per channel	1 GSa (500 MSa I and 500 MSa Q)
Number of waveforms, per channel	4096
DAC output sample rate	38.4 GSa/s
Minimum waveform length, per channel	64 Samples (I+Q), 13.3 ns
Maximum waveform length, per channel	1 GSamples (I+Q), 223 ms
NCO frequency coverage	0-18 GHz
NCO Frequency resolution	5×10^{-6} Hz
NCO Phase resolution	84×10^{-9} degrees
Noise floor (NSD)	-157 dBm/Hz
Phase noise [4]	-130 dBc/Hz at 8 GHz,10 kHz offset -125 dBc/Hz at 16 GHz, 10 kHz offset
Channel to channel isolation	80 dB to 16 GHz
Spurious Free Dynamic Range (SFDR) Excluding harmonics and DAC interleave spurs	-70 dBc to 16 GHz
Spurious Free Dynamic Range (SFDR) Excluding harmonics, including DAC interleave spurs [5]	-55 dBc to 16 GHz

[4] When used with M9046A-QS1
[5] Including DAC interleave spurs near 9.6 GHz

Module power requirements

Total power dissipation	50 W [6]	
Supply voltage	+3.3 V	+12 V
Supply current	6.3 A	2.4 A

Clock and I/O characteristics

Module reference clock	
Clock sources	Front panel, PXI_CLK100
Front panel clock frequency	2.4 GHz
Nominal input clock power	+15 dBm
Module self-clocking	Yes
Accuracy	Chassis dependent
Input/output triggers	
Trigger sources	Software, PXI_TRIG, PXI_STAR, and front panel I/O
Trigger destinations	PXI_TRIG and front panel I/O
Trigger polarity	Active high or active low (programmable)
Trigger jitter	100 ns
Max PXI trigger toggle rate	100 MHz

Trigger channel characteristics

Number of channels	8
Channel type	Single-ended, bidirectional, ground reference
Default state	1 MΩ nominal, input
Output characteristics (typical)	
Ouput voltage 50 Ω load High impedance load	 0 V - 1.6 V 0 V - 3.2 V
Maximum output channel toggle rate	150 MHz
Input characteristics (typical)	
Input voltage range	0 - 5 V
Maximum low voltage threshold	0.8 V
Maximum high voltage threshold	2 V
Load impedance	1 MΩ
Maximum input channel toggle rate	75 MHz

FPGA characteristics

FPGA type	Xilinx Virtex Ultrascale+ (XCVU35P)
FPGA sandbox size	1/6 of FPGA resources
Timebase frequency	300 MHz (phase-locked to 100 MHz chassis clock)
Timebase source	PXI_CLK100 or DSTARA

[6] Nominal power without application specific gateware

FPGA resource estimates

Site type	Available	Used	% Utilized	Available to user
CLB LUTs	244936	9424	3.85	235512
LUT as logic	244936	9369	3.83	235567
LUT as memory	113192	55	0.05	113137
CLB registers	489872	10028	2.05	479844
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Register as latch	489872	0	0	489872
CARRY8	30617	162	0.53	30455
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CLB	30617	3647	11.91	26970
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CLBM	14149	1676	11.85	12473
Unique control sets	61234	1144	1.87	60090
Block RAM tile	360	0.5	0.14	359.5
RAMB36/FIFO	360	0	0	360
RAMB18	720	1	0.14	719
URAM	240	0	0	240
DSPs	1872	0	0	1872

M5302A characteristics

General characteristics

Description	PXIe Digital I/O
Bus interface and compatibility	PXIe peripheral module (x8 Gen 3)
Number of slots	1
Volatile module memory	8 GB (DDR4)
Non-volatile flash memory	1 GB
Front panel connectors	
LVDS	ERF8-050
Trigger channels	SMB male (8)
System sync	Reserved for future use
Mechanical (nom)	
Size	3U/1-slot PXIe standard 130.1 x 21.7 x 210 mm; includes connectors and handle extensions
Weight	365 g (0.8 lb)

Module power requirements

Total power dissipation	42 W	
Supply voltage	+3.3 V	+12 V
Supply current	1.8 A	3 A

LVDS connector characteristics

Channels	
Functionality	LVDS plus auxiliary DUT power supply
Channel type	Differential, bidirectional
Number of channels	28
Channel impedance	100 Ω differential (nominal)
LVDS output characteristics (typical)	
Output voltage range	1.25 V ± 175 mV (100 Ω differential termination)
Maximum output short circuit current	20 mA
Maximum output channel toggle rate	1.2 Gbps
LVDS input characteristics (typical)	
Differential input voltage range	0.3 - 1.4 V (DC coupled) 0.6 - 1.1 V (AC coupled)
Input common mode voltage threshold	0.1 - 0.6 V
Maximum input toggle rate	1.2 Gbps

LVDS channel skew characteristics (typical) [7]	
Maximum skew adjustment range	±1667 ps (user) + ±1667 ps (system) = ±3333 ps (total)
Maximum skew adjustment resolution	50 ps
Maximum edge polarity skew	±50 ps
Maximum uncalibrated inter-channel skew error [8,9]	±150 ps
Maximum inter-channel skew drift (±5 ˚C)	±200 ps
Input/output triggers	
Max uncalibrated inter-module skew error [10,11]	±250 ps
Maximum inter-module skew drift (±5 ˚C)	±300 ps
HVI action/event time resolution	3.33 ns

DUT power supply (typical)	
Output voltage	5 V ±5%
Maximum output current	0.5 A

Trigger channel characteristics	
Number of channels	8
Channel type	Single-ended, bidirectional, ground reference
Default state	1 MΩ nominal, input
Output characteristics (typical)	
Ouput voltage 50 Ω load High impedance load	 0 V - 1.6 V 0 V - 3.2 V
Maximum output channel toggle rate	150 MHz
Input characteristics (typical)	
Input voltage range	0 - 5 V
Maximum low voltage threshold	0.8 V
Maximum high voltage threshold	2 V
Load impedance	1 MΩ
Maximum input channel toggle rate	75 MHz

7 Note that a 1.2 GBps data valid window = 833 ps
8 Total uncalibrated skew error between any two channels on same module over ±5 ˚C ≤ 2 x (Max Uncalibrated Inter-Channel Skew Error + Max Inter-Channel Skew Drift + Max Edge Polarity Skew) = 800 ps
9 Total user-calibrated skew error between any two channels on same module over ±5 ˚C ≤ 2 x (Max Skew Adjustment Resolution / 2 + Max Inter-Channel Skew Drift + Max Edge Polarity Skew) = 550 ps
10 Total uncalibrated skew error between any two channels across separate modules over ±5 ˚C ≤ 2 x (Max Uncalibrated Inter-Module Skew Error + Max Inter-Module Skew Drift + Max Edge Polarity Skew) = 1200 ps
11 Total user-calibrated skew error between any two channels across separate modules over ±5 ˚C ≤ 2 x (Max Skew Adjustment Resolution / 2 + Max Inter-Module Skew Drift + Max Edge Polarity Skew) = 750 ps

Trigger channel skew characteristics (typical) [12]

Maximum skew adjustment range	±1667 ps (user) + +/-1667 ps (system) = ±3333 ps (total)
Maximum skew adjustment resolution	50 ps
Maximum edge polarity skew	±250 ps
Maximum uncalibrated inter-channel skew error [13,14]	±500 ps
Maximum inter-channel skew drift (±5 ˚C)	±200 ps
Performance with Option KS2201A	
Max uncalibrated inter-module skew error [15,16]	±250 ps
Maximum inter-module skew drift (±5 ˚C)	±300 ps
HVI action/event time resolution	3.33 ns

Module timing and trigger characteristics

Module reference clock	
Frequency	100 MHz
Reference clock source	PXI_CLK100
Accuracy	Chassis dependent
Input/output triggers	
Trigger sources	Software, PXI_TRIG, PXI_STAR, and front panel I/O
Trigger destinations	PXI_TRIG and front panel I/O
Trigger polarity	Active high or active low (programmable)
LVDS input characteristics (typical)	
Differential input voltage range	0.3 - 1.425 V (DC coupled) 0.6 - 1.1 V (AC coupled)
Input common mode voltage threshold	0.1 - 0.6 V
Maximum input toggle rate	1.2 Gbps

FPGA characteristics

FPGA type	Xilinx Virtex Ultrascale+ (XCVU35P)
FPGA sandbox size	1/6 of FPGA resources
Timebase frequency	300 MHz (phase-locked to 100 MHz chassis clock)
Timebase source	PXI_CLK100 or DSTARA
Available FPGA resources	
CLB registers	502320
CLB LUTs	251160
Block RAM tiles (Mb)	480
UltraRAM (Mb)	80
DSP blocks	960

12 Note that a 300 Mbs Gbps data valid window = 3333 ps
13 Total uncalibrated skew error between any two channels on same module over ±5 ˚C ≤ 2 x (Max Uncalibrated Inter-Channel Skew Error + Max Inter-Channel Skew Drift + Max Edge Polarity Skew) = 2500 ps
14 Total user-calibrated skew error between any two channels on same module over ±5 ˚C ≤ 2 x (Max Skew Adjustment Resolution / 2 + Max Inter-Channel Skew Drift + Max Edge Polarity Skew) = 1550 ps
15 Total uncalibrated skew error between any two channels across separate modules over ±5 ˚C ≤ 2 x (Max Uncalibrated Inter-Module Skew Error + Max Inter-Module Skew Drift + Max Edge Polarity Skew) = 3500 ps
16 Total user-calibrated skew error between any two channels across separate modules over ±5 ˚C ≤ 2 x (Max Skew Adjustment Resolution / 2 + Max Inter-Module Skew Drift + Max Edge Polarity Skew) = 2050 ps

Ordering Guide and Upgrade Information

Contac your Keysight representative or authorized partner for more information, or to place an order: www.keysight.com/find/contactus

Cabling

When configuring with the M9046A-QS1 option, all cables must be the same length to ensure proper functioning of the clocking mechanism.

Model	Description
Y1320A	System Sync/Link cable, x4-x4, 0.5m
Y1321A	System Sync/Link cable, x4-x4, 1.0m
Y1323A	System Sync/Link cable, x8-2, x4, 0.5m
Y1324A	System Sync/Link cable, x8-2, x4, 1.0m
Y1326A	System Sync/Link cable, x8-x8, 0.5m
Y1327A	System Sync/Link cable, x8-x8, 1.0m
Y1329A	System Sync/Link cable, x8-x8, 2.0m
71330A	MCX(m) to MCX(m) cable, phase stable, 0.3m
Y1331A	MCX(m) to MCX(m) cable, phase stable, 1.0m
Y1332A	MCX(m) to MCX(m) cable, phase stable, 2.0m
Y1333A	SMA(m)-SMP(f) cable, 0.3m

Software options

Model	Description
M5401LUNA	Labber Quantum Software License
KS2201A	PathWave Test Sync Executive License
KF9001B	PathWave FPGA Run Time License
M5400B	Quantum FPGA IP Library for M5xxx Control Hardware

For more information

For more insights on how to accelerate innovation in quantum computing, visit the Quantum Control System Solution Brief.

To combine additional PXIe products, visit our PXI Product Portfolio.

For more information on software offerings, visit PathWave FPGA, PathWave Test Sync Executive, and Labber.