M5400DMOA

Quantum Library Demodulation

Overview

The M5400DMOA allows quick and easy access to targeted quantum signal processing FPGA IP blocks used within PathWave FPGA to complete an entire demodulation IQ path with customizable configurations that include real-time sequenced triggering, digital down-sampling and custom filtering, qubit state detection and multi tone capable IQ data memory management all designed and optimized to be used with the M3102A real time control hardware platform.

The M5400DMOA software package

This licensed software package for the quantum library includes a quantum M5400DMOA programming API that directly interacts the SD1 3.X driver communication, KS2201A PathWave Test Sync Executive and Quantum FPGA IP library for a user friendly programming environment that can quickly be used for qubit control and readout applications.

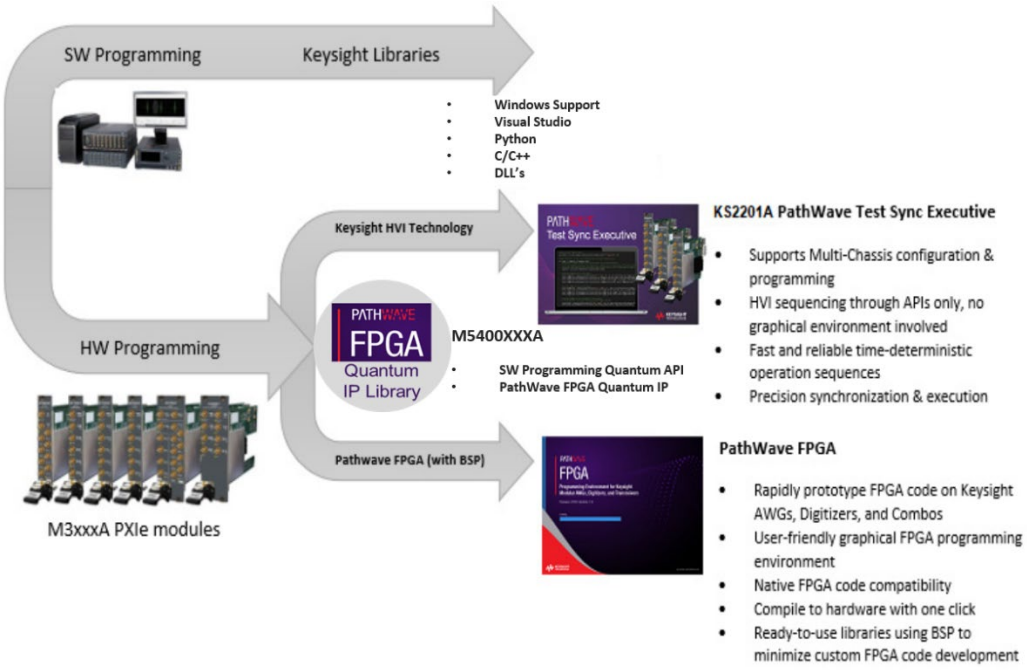

Figure 1. M5400DMOA operation flow

Using the fully integrated software and FPGA Gateware package allows for simplifying your configuration and provides massive savings of development time to integrate and expand to multi qubit systems including multi-chassis configurations for scaling system configurations.

What is included?

Feature	Description	Includes	Licensing
M5400DMOA	Quantum Library Demodulation	Quantum Library API, PathWave FPGA Quantum IP Library	Run-time per PXIe Instrument Module

Features

The Quantum FPGA IP provides ultra-light weight and scalable components that have a small FPGA footprint that allows for frequency division multiplexing capable for multi qubit readout. The convenient quantum FPGA IP provides the ability to phase lock to the M320xA AWG with no external references required. Using precise real-time control through PathWave Test Sync Executive technology known as HVI, hardware virtual instrument, allows for deterministic triggering that is synchronized with the M320XA PXIe instrument AWG.

- DDC - Digital downconverter with custom programmable dual LO that is phase adjustable to rotate and accommodate IQ constellations.
- Digital Downsampler with customizable integrating rectangular or customer filter windows including decimation.
- Qubit Decoder for qubit state discrimination for active |1> or ground state |0> through amplitude and phase detection using a single threshold detection technique from a single IQ point readout pulse result.
- Data Wrappers that handle data management of IQ and state data for up to 16 qubits on a single M3102A PXIe module.

Table 1-1: Technical Performance Specifications (IP Components)

IP Component	Nominal Characteristics					
	Parameter	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
DDC						
	Frequency	0		200	MHz	5.68 µHz resolution; 45 bits
	Phase	-180		180	degree	21.5 µdegree resolution; 24 bits

IP Component	Nominal Characteristics					
	Parameter	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
DownsamplerX5N						
	Filter Type	rectangular		custom	window	rectangular (average) custom (time-based coefficients)
	Rectangular Length	10		65535	samples	20 ns to 1.31 ms; 5 ns increments
	Custom Length	10		10240	samples	20 ns to 20 µs; 5 ns increments
	Latency		10		ns	after readout pulse
Qubit Decoder						
	Threshold	-1.5		1.5	Volts	DC threshold applied after demodulation filter window
	Latency		10		ns	after downsampler
DataWrapperXN						configurations support IFIQ on single channel or IQ baseband inputs across two channel inputs
	Cycles	1		3x1e6	cycle	Supports up to 3M triggers of IQ and state data samples per qubit
	Custom Filter	1		16	qubits/module	IQ IFIQ configuration across 4 channels. See utilization table below
	Rectangular	1		8	qubits/module	IFIQ configuration across 2 channels. See utilization table below

Table 1-2: Technical Performance Specifications (Sandbox Interfaces)

Sandbox Interfaces	Nominal Characteristics					
	Parameter	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
Sampling Clock	Clock		100		MHz	5 samples/clk (10 ns)
System Reset	nRst		10		ns	active low sandbox system reset

Only key parameters listed in the Tables; not all inclusive: Only key quantum IP components have been listed in Table 1-1 and Table 1-2. Many other complementing IP components are included in the quantum IP library. Many sandbox interfaces and off-the-shelf IP components included with PathWave FPGA are not listed here.

Table 2: Utilization Data

Limiting Factors	Utilization			
IF IQ Demodulation Resource Considerations -k41 target 4 Channel M3102A				
Component	**BRAM**	**DSP**	**LUT**	**Notes**
DownsamplerX5N	5	6	76	Rectangular Window IF IQ
DataWrapperXN	1	0	297	DataWrapperX4
DDC	5	68	961	Digital Down Converter
Qubit Decoder	0	0	111	Qubit Decoder
1 channel IF IQ Qubit demodulation path	15	80	1224	x2 Downsamplers x1 DDC x1 Qubit State x1 DataWrapperX4 (not included in totals)
Channel Configurations (330 BRAM max, 660 DSP max per -k41 playground)				
8 Qubit (2 channels)	122	640	10,386	qnt 2 DataWrapperX4 (included in totals)
IQ Demodulation Resource Considerations -k41 target 4 Channel M3102A				
Component	**BRAM**	**DSP**	**LUT**	**Notes**
DownsamplerX5N	5	6	76	Custom Window; matched coefficients
DataWrapperXN	1	0	297	DataWrapperX5, X4 options
Adder/Subtract	0	0	87	Adder/Subtractor
2 channel IQ IFIQ 1-Qubit demodulation path	20	24	478	Channel 1 - I input Channel 2 - Q input x4 DownsamplerX5N x2 Adder/Subtract X1 DataWrapperXN (not included in totals)
Channel Configurations (330 BRAM max, 660 DSP max per -k41 playground)				

Limiting Factors	Utilization			
10 Qubit (2 channels)	202	240	5374	assumes qnt 2 DataWrapperX5 (included in totals)
15 Qubit (4 channels)	303	360	8061	assumes qnt 3 DataWrapperX5 (included in totals)
16 Qubit (4 channels)	324	384	8836	assumes qnt 4 DataWrapperX4 (included in totals)

PathWave FPGA Use Model

Create custom FPGA designs within your own partitioned FPGA space known as a "sandbox" within a supported PathWave FPGA enabled PXIe instrument.

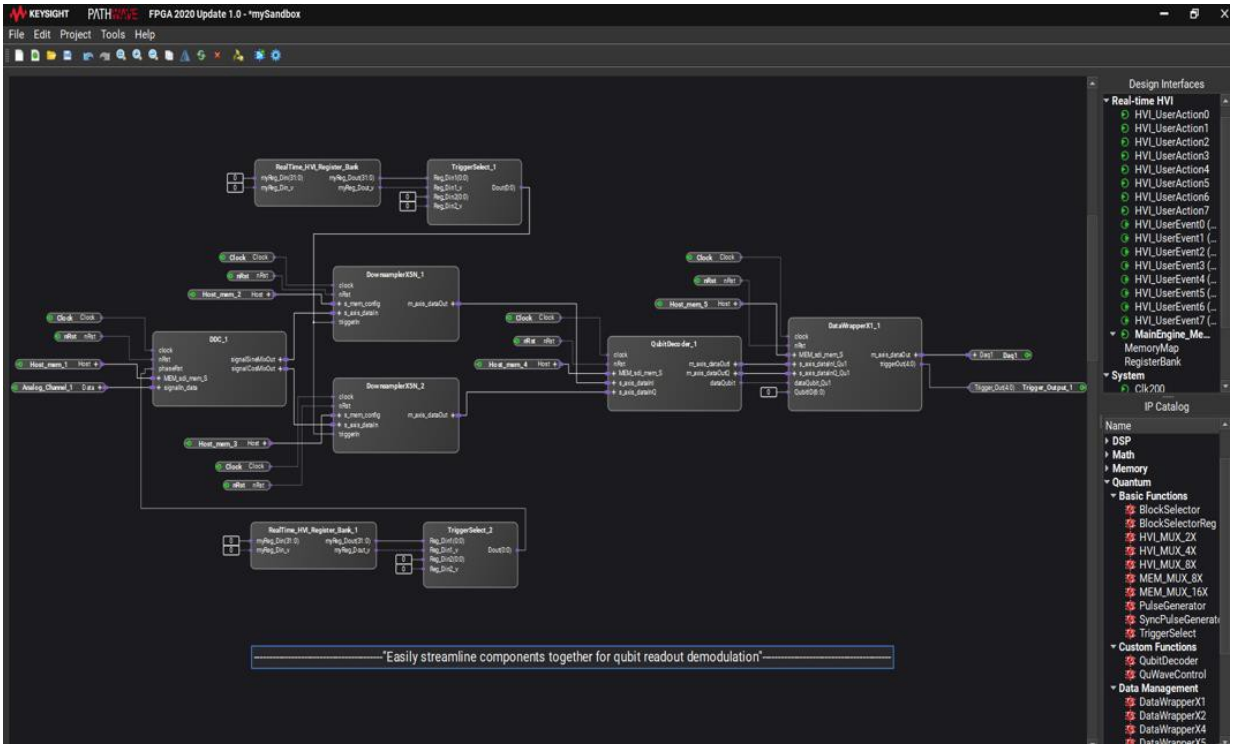

Figure 2. PathWave FPGA use model

You can easily integrate ready to use off-the-shelf custom quantum FPGA IP blocks to create readout demodulation for many qubits in a single schematic with no Gateware HDL programming knowledge required.

Procurement information

Products	Model Number
M5400DMOA Demodulation	M5400DMOA
Dependencies	
KS2201A PathWave Test Sync Executive	KS2201A
KF9000A PathWave FPGA Programming Environment	KF9000A
M3102A PXIe Digitizer 500MSa/s, 14 bit, 200 MHz -K41 -HV1 CLF (SD1 3.X driver)	M3102A

Licensing terminologies

Terminology name	Description
Subscription	Subscription licenses can be used through the term of the license only (6, 12, 24, or 36 months).

Licensing types

License type	Description
Node-locked	License can be used on one specified instrument/computer.
Transportable	License can be used on one instrument/computer at a time but may be transferred to another using Keysight Software Manager (internet connection required).
USB Portable	License can be used on one instrument/computer at a time but may be transferred to another using a certified USB dongle (available for additional purchase with Keysight part number E8900-D10).
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