DATA SHEET

M8062A 32 Gb/s Front-End for J-BERT M8020A High-Performance BERT

Version 4.0

KEYSIGHT TECHNOLOGIES

Introduction

The M8062A extends the data rate of the J-BERT M8020A Bit Error Ratio Tester to the speeds required for testing devices with lane rates in the 25-28 Gb/s range. When combined with a two channel M8041A, the system provides data pattern generation and full rate error analysis for users developing 100G class serial data link components and systems with lane rates up to 32.4 Gb/s.

Typical applications:

- Receiver characterization and compliance test
- 100G Serdes (CAUI-4)
- OIF CEI 19-28 Gb/s electrical interfaces
- Backplane receivers for IEEE 802.3 100GBASE-KR4 and 25GBASE-KR
- Optical Transceiver modules and sub-components for IEEE 802.3 100GBASE-SR4, LR4, and -ER4, 32G Fibre Channel, SAS 24G
- Thunderbolt 3 (20 Gb/s)
- Active Optical Cables

Key Features

- Extends maximum data rate of J-BERT M8020A up to 32.4 Gb/s
- Jitter injection built-in and calibrated (LFPJ, HF PJ, Clk/2, BUJ, RJ, SSC)
- Integrated 8-tap de-emphasis up to 24 dB to emulate TX de-emphasis
- Built-in ISI generator for channel emulation
- Interference injection (common mode and differential mode) from single ended source
- Clean clock output with selectable dividers
- Built-in clock recovery
- Analyzer equalization eliminates errors resulting from closed eyes in loop back path
- TX Equalizer Negotiation for 100GBASE-KR4 and 25GBASE-KR
- Secure investment - options are upgradeable later

Accurate Characterization and Compliance Testing 100G Class Devices and Systems

With a data rate of up to 32.4 Gb/s, the M8062A with the J-BERT M8020A has the speed required to address 100G class serial links used in data center networking applications, as well as emerging higher speed computer bus standards such as Thunderbolt 3 and SAS 24G. In addition to supporting all of the stress types required for compliance testing to these standards, the system offers several features that greatly improve efficiency and accuracy when performing characterization tests.

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Get Accurate Results Based on M8062A's Excellent Output Performance

The eye quality of the pattern generator output is critical when characterizing many pass through devices such as TOSAs. The low intrinsic random jitter assures that you will be measuring the true performance of the device under test itself. Fast transition times preserve the eye opening at the highest data rates, maintaining margins for repeatable BER measurements.

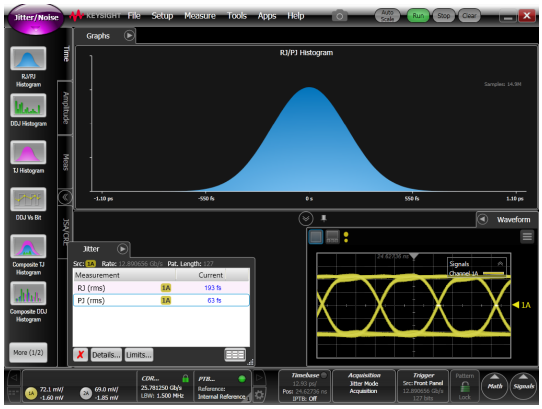

Figure 1. Intrinsic RJ < 200 fs

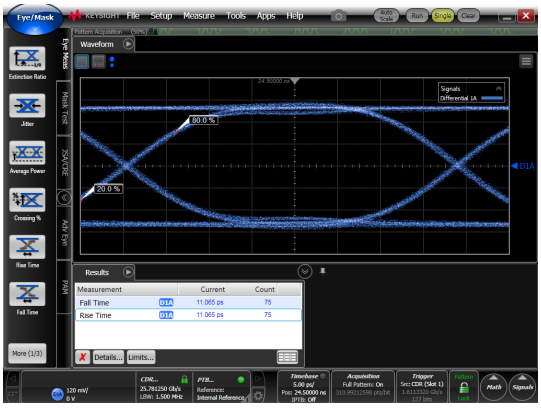

Figure 2. Output eye showing rise time < 12 ps.

Emulate Channel Loss with Integrated and Adjustable Inter-Symbol Interference

Most receivers designed for applications with lane rates of 25 - 28 Gb/s contain equalization to counter the effects of channel loss. The equalization design may be a multi-step continuous time linear equalizer (CTLE), or a combination of CTLE and decision feedback equalizer (DFE). Many devices include auto-optimizers which select the optimum equalization settings during a training cycle. To verify the design, the receiver must be tested with a variety of channels to create various amounts of eye closure. Because these designs have multiple CTLE gain or DFE tap settings, design verification requires inclusion of channel losses in the middle of the operating range, rather than just the minimum and maximum.

Traditionally, testing with a variety of channel losses was a tedious process, requiring changing cables between connectors on test trace boards which emulate various channel lengths. Using this method, the resolution in channel loss is limited. The potential for an auto-optimizing design to fail to converge at a particular intermediate channel loss may not be discovered during characterization testing, if the particular loss which causes the problem lies between the fixed lengths of test channels being used.

The M8062A overcomes both of these problems by offering an electronically adjustable ISI generator, for emulating channel loss. The M8062A adds electronic filters in the pattern generator data stream. The user can set one or two frequency breakpoints, and select the insertion loss value at each, providing continuously adjustable frequency dependent loss to emulate the channel. By eliminating the need to manually move cables, characterization testing of receiver equalization becomes much more efficient.

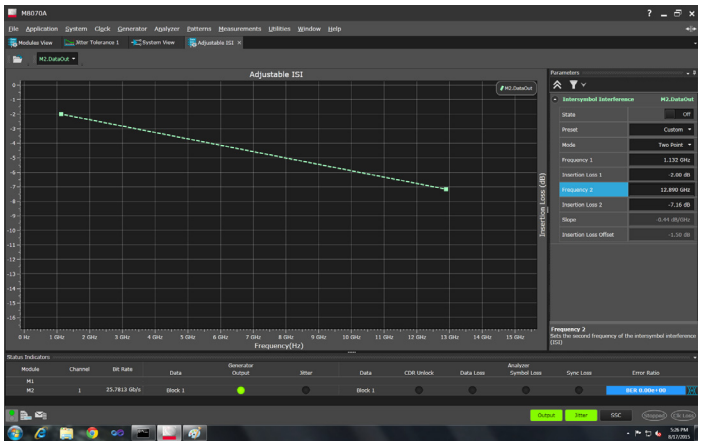

Figure 3. Control ISI for channel emulation is simply entering loss and frequency breakpoints, or by Importing S-parameters.

Emulate Transmitter De-Emphasis and Compensate for Channel Loss

Virtually all transmitters 25 - 28 Gb/s lane rates include multi-tap de-emphasis. The M8062A 32 Gb/s BERT front-end offers integrated 8 tap de-emphasis, to emulate the system transmitter, or simply de-embed the cables and test fixtures from the test set-up.

Up to 8 taps can be configured as 5 post cursor, and 2 pre-cursor. Tap weights are individually settable, with essentially no interaction.

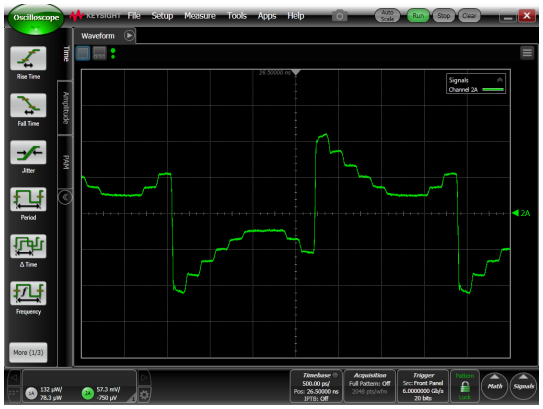

Figure 4. De-emphasis capability is built into the M8062A, not requiring external signal processing boxes" which add cables and complicate the test set-up

Analyze Bit Errors on Closed Eye with Integrated Analyzer Equalization

In a receiver test setup, the receiver under test is fed a test pattern from the pattern generator, and the received signal is looped back and re-transmitted to the BERT error analyzer. The loopback channel is not "stressed" to preserve the eye quality for accurate BER measurements.

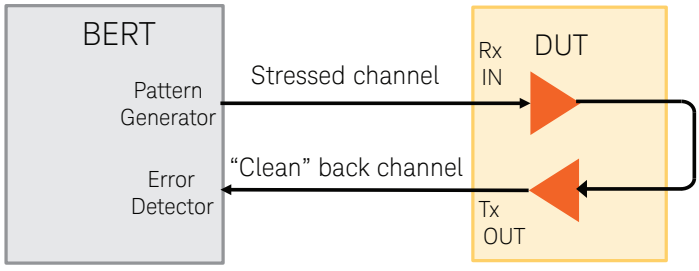

Figure 5. Typical BERT test setup

At data rates above 20 Gb/s, even the clean back channel which feeds the BERT error analyzer will have some eye closure caused by the channel loss. ISI in the back channel can cause errors in the error analyzer when the eye is closed excessively, resulting in overstated bit errors.

Adding equalization capabilities to the input of the error analyzer opens partially closed eyes in the back channel, ensuring only the receiver errors from the device under test are considered in the BER measurement.

Simplify Test Set-Up With Integrated Level Interference Injection

For applications which inject interference before the channel, built-in superposition eliminates the need for external power splitters. Front-panel connectors allow superposition of external interference sources such as sine wave generators or random noise sources directly into the pattern generator data. Both common mode and differential mode injection paths are provided. The Common Mode is added at the end of the ISI channel, whereas the Differential Mode is injected before. See figure below.

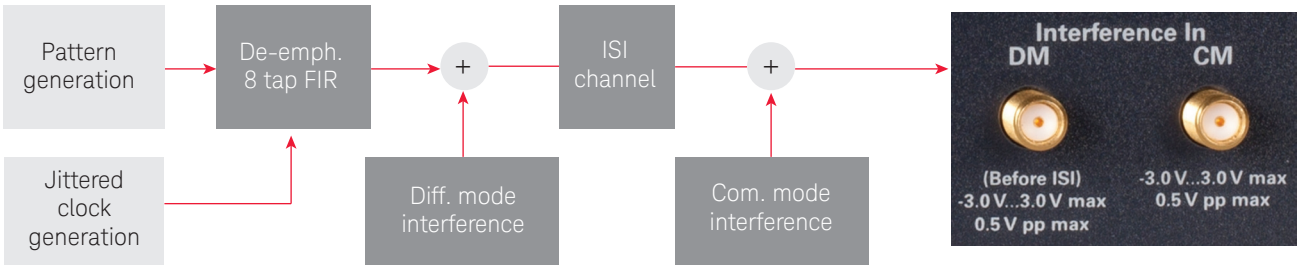

Figure 6. Block diagram for pattern generator with external distortion sources Input connectors for level interference (on the right side).

Analyze Clock-Less Devices by Using the Built-In Clock Data Recovery

The clock for the error analyzer can be sourced from the pattern generator clock, a user supplied external clock, or directly from the data with the optional clock recovery. High loop bandwidth is able to track pass through jitter from virtually any device being tested.

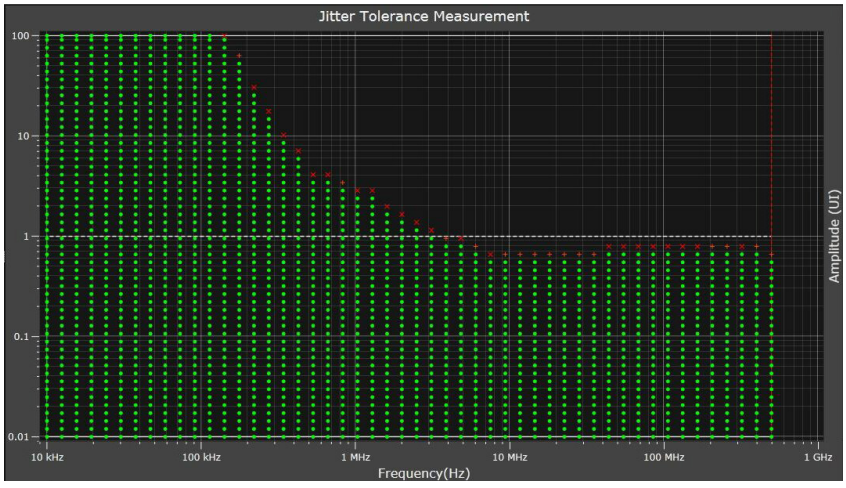

Figure 7. Example jitter tolerance performance using internal Clock Data Recovery

Automated Jitter Tolerance Measurements Up to 32 Gb/s

The M8062A front-end can be used to provide automated jitter tolerance measurements up to 32 Gb/s with J-BERT M8020A. The built-in jitter sources can be swept over the modulation frequency range. Jitter tolerance masks can be setup with the template editor easily. Results can be exported.

Specifications 32 Gb/s Pattern Generator

Pattern generator data out	
Output data rate	512 Mb/s to 32.4 Gb/s, using M8041A internal clock
Channels	1
Data format	Non-Return to Zero (NRZ), single ended and differential
Output amplitude	0.05 Vpp to 1.2 Vpp (single ended) 0.1 to 2.4 Vpp (differential) Output from 50 Ω source. Output amplitude values calibrated only when driving a 50 Ω load. See next table for max output amplitude if offset is > 1.9 V or CMI/DMI are turned on.
Output amplitude resolution	1 mV (single-ended)
Voltage window	–1 V to +3 V
External termination voltage	–1 V to +3 V For offset > 1.3 V, the termination voltage must be within ±0.5 V of the offset voltage
Transition times	12 ps typical (20%/80%)[1]
Intrinsic random jitter	< 200 fs rms typical, data rates 20.625 – 32.0 Gb/s[2]
Total jitter	6 ps pp typical, data rates 20.6 – 30.0 Gb/s at a target BER of 10^{-12}
Adjustable Inter-symbol Interference (ISI)	Linear loss curve to one or two settable breakpoints: Loss: 0.5 dB – 25 dB (upper point), 1.5 dB – 25 dB (lower point) Frequency: 1 – 16.2 GHz
Crossing point	Adjustable from 30% to 70% nominal
Electrical idle transition time	Output transitions from full swing signal to 0 V amplitude and vice versa at constant offset within 4 ns typical.
Jitter pass through	All jitter sources in the M8041A pass through the M8062A transparently except clock/2 jitter and adjustable ISI, which are generated within the M8062A. The upper range of pass through jitter generally doubles, while the resolution halves. Maximum jitter amplitude may be limited at data rates above 18 Gb/s.
Clock/2 (Even/Odd) jitter injection range	Up to ±0.1 UI or ±20 ps (whatever is less). This means that first eye can be up to ±0.1 UI (or 20 ps) longer or shorter than the subsequent eye.
Termination impedance range	To protect the output stage, the output is disabled when an unexpected voltage or termination impedance is detected. DC output coupling mode: Termination range for devices connected to data out: – Unbalanced 50 Ω +15 Ω /-10 Ω – Typical balanced 100 Ω ± 30 Ω typical Operation into open is possible for these ranges when “DC coupled“ and “balanced“ termination modes are selected: – output amplitude max. 300 mV [4] – offset 0 to 370 mV AC coupling mode: When using the AC coupled mode you must apply an external DC blocking capacitor is expected. The external DC resistance must be greater than or equal to 300 Ω, with the HF resistance being ~50 Ω (single-ended) or ~100 Ω (differential).
Connectors	2.4 mm female

1. Measured with an oscilloscope with at least 50 GHz BW, such as DCA-X with 86108B plug-in. Measured single ended at 900 mV output amplitude.
2. Measured with PRBS-15 pattern, using oscilloscope with < 50 fs rms intrinsic jitter, such as DCA-X with 86108B plug-in set for 50 GHz BW mode and using internal precision time base.
3. Per output when differentially terminated into 100 Ω. Results in doubled swing when driving into open.

Specifications 32 Gb/s Pattern Generator (continued)

Data output amplitude maximum in presence of Common Mode Interference (CMI) and/ or Differential Mode Interference (DMI), offset voltage

CMI	DMI	Offset ≤ 1.9 V	Offset > 1.9 V
Disabled	Disabled	1.2 V	0.9 V
Disabled	Enabled	0.9 V	0.675 V
Enabled	Disabled	0.9 V	0.75 V
Enabled	Enabled	0.675 V	0.5625 V
Enabled	Enabled[1]	0.8 V	0.666

1. For DMI < 12.5 % of amplitude.

De-emphasis of data out (option 0G4)	
De-emphasis taps	8, 2 pre-cursor, 5 post-cursor
Pre-cursor 2 range	±6.0 dB
Pre-cursor 1 range	±12.0 dB
Post-cursor 1 range	±20.0 dB
Post-cursor 2 range	±12 dB
Post-cursor 3 range	±6 dB
Post-cursor 4 range	±6 dB
Post-cursor 5 range	±6 dB
De-emphasis tap resolution	0.1 dB

Note: Output amplitude will be scaled as necessary such that Output Amplitude Vpp setting is not exceeded as a result of cursor settings

Pattern generator clocks (half rate)	
Frequency range	256 MHz to 16.2 GHz
Clock out amplitude	0.75 V pp nominal, single ended
Clock out interface	AC coupled, 50 Ω nominal
Aux clock input	For alternate clock input must be synchronous with M8041A clock.
Aux clock input amplitude range	0.2 to 1.0 V pp, nominal
Aux clock input minimum transition time	< 200 ps
Clean clock out amplitude	300 mV pp nominal
Clean clock out divide ratios	1, ... N, from 256-16 GHz 2, ... N, even only, from 16-16.2 GHz The maximum value of N is limited such that the clean clock out frequency is ≥ 2 MHz
Clean clock out interface	AC coupled, 50 Ω nominal
Clock connectors	3.5 mm female

CMI/DMI in, electrical idle in	
CMI/DMI max. Input Voltage	±400 mV single ended, nominal
Common mode interference (CMI) input (Injected after ISI emulation, at output)	0 to 400 mV, corresponds to gain range 0 to 1 10 MHz to 1 GHz
Differential mode interference (DMI) input (injected before ISI emulated channel)	0 to 30% of output amplitude, corresponds to gain range 0 to 1 10 MHz to 6 GHz
EIDL input threshold voltage	–1 to +3 V
EIDL input termination voltage	–1 to +3 V
EIDL input termination voltage accuracy	±(35 mV + 1%)
Connector	3.5 mm female

Specifications 32 Gb/s Error Analyzer

Analyzer data in	
Data rate	512 Mb/s to 32.4 Gb/s, using system clock 1 Gb/s to 32.4 Gb/s using external clock 2 Gb/s to 32.4 Gb/s using internal clock recovery Analyzer data rate must be within ±50 ppm of pattern generator data rate.
Channels	1
Data format	NRZ, single ended or differential
Input sensitivity	50 mV, min. differential, typical, in High Sensitivity mode[1]
Maximum swing	1.6 Vpp differential
Input interface	100 Ω differential, 50 Ω single ended, AC coupled
Clock-to-data delay timing resolution	1 ps[2]
Input connectors	2.4 mm, female

1. Using PRBS-31 pattern
2. Clock-to-data adjustment not available when analyzer operates under internal CDR mode

Analyzer equalizer	
Equalization	Allows recovery of data from partially closed eyes resulting from frequency dependent loss, for BER measurement. Available at data rates 20.0 Gb/s and higher.
Gain range	Up to 9 dB at 16 GHz
Configuration	CTLE with true differential topology (no skew is introduced)

Analyzer clock in (half rate)	
Frequency range	500 MHz to 16.2 GHz, must be within ±50 ppm of pattern generator data rate / 2
Input voltage amplitude range	0.25 to 1.0 Vpp, nominal
Interface	AC coupled, 50 Ω, nominal
Connector	3.5 mm, female

Analyzer clock out (Half data rate clock output from the selected analyzer clock source)	
Amplitude	± 0.5 - 1.2 Vp-p from 50 Ω source
Frequency range	4.2 - 16.2 GHz. At clock rates below 4.2 GHz, output signal may have excess jitter

Clock recovery (option)	
PLL characteristics	2nd order, fixed LBW 25 MHz with no measureable peaking
Data rate range	1-32.4 Gb/s
Input sensitivity	50 mV Vpk-pk diff., typical
Minimum transition density	20%
Spread spectrum clock tracking	5300 ppm @ 36 kHz down spread, data rate = 20.625 Gb/s 100 ppm center spread, data rate = 22.5 Gb/s

Specifications 32 Gb/s Module and Interface

Module user interface and remote control interface	
BERT system software	M8070B
External controller	PCIe connectivity: Please refer to list of tested PCs in the technical note: 5990-7632EN USB connectivity
Connectivity AXIe chassis	USB 3.0, PCIe 2.0 / 8x
Programming interface	SCPI

General characteristics	
Operating temperature	5 to 35 °C
Storage temperature	–40 to 70 °C (Module only)
Operating humidity	15% to 95% relative humidity at 40 °C (non-condensing)
Storage humidity	24% to 90% relative humidity at 65 °C (non-condensing)
Power requirements (module only)	117 W, typical
Physical dimension (W x H x D)	Module in a 5-slot AXIe chassis 143 x 194 x 446 mm: (5.64” x 7.64” x 17.56”)
Weight	4.1 kg (9.0 lb.), module only
Recommended recalibration interval	1 year

Ordering Information

Product options	
Options are field upgradeable except for -0A4 [1]	
M8062A-C32	32 Gb/s BERT front-end
M8062A-G32	32 Gb/s Pattern generator front-end
M8062A-0G4	8-tap de-emphasis license
M8062A-0G5	Adjustable inter-symbol interference license
M8062A-0A3	Analyzer equalization license[2]
M8062A-0A4	Clock recovery up to 32 Gb/s[1]
M8062A-0S6	SAS-3/SAS-4 transmitter equalization training[2]
M8062A-0SC	100GBASE-KR4 and 25GBASE-KR transmitter equalization training[2]
M8062A-US6	Upgrade of M8041A to SAS-3 transmitter equalization training
M8062A-0SC	100GBASE-KR4 and 25GBASE-KR transmitter equalization training, module-wide license

1. This option is field upgradeable for units with serial number higher than MY55400300. Units with a lower serial number require return to factory for this upgrade.
2. Requires option M8062A-0G4 to allow de-emphasis negotiation.

Recommend configuration for 32 Gb/s BERT:

- M8020A-BU5 5 slot AXIe chassis configured with M8041A,
- M8041A-C16, M8041A-0A2, M8041A-0G2 BERT configured with two channels,
- M8070B-BER test system software.

The M8062A includes the following accessories by default: M8041A interconnect cable set, sync cable, 3 50 Ω terminators, and commercial calibration report.

Other recommended accessories	
Matched cable pair, 2.4 mm, 85 cm long (for connecting Data Out/Data In to DUT)	N4910A
DC block, 50 GHz (insert in Data Output when driving single ended AC coupled input)	N9398F
6 dB attenuator, 50 GHz (Use to protect sampling scope input when monitoring Data Output)	8490D
Rack-mounting kit for AXIe 5 slot chassis	Y1226A

Replacement parts	
Replacement Sync cable	M8062A-801
Replacement cable set, semi-rigid, Pattern Generator	M8062A-802
Replacement cable set, semi-rigid, Error Analyzer	M8062A-803

Related Keysight literature	
J-BERT M8020A High Performance Serial BERT – Data Sheet	5991-3647EN
J-BERT M8020A – Configuration Guide	5991-4032EN
M8061A 32 Gb/s Multiplexer with De-Emphasis - Data Sheet	5991-2506EN
Characterizing and verifying compliance of 100 Gb Ethernet components and systems – Application Note	5992-0019EN
M8030A Multi-channel BERT - Data Sheet	5992-1287EN
M8040A High-Performance BERT 64 GBaud - Data Sheet	5992-1525EN

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