DATA SHEET

M8131A – 16/32 GSa/s Digitizer

Data Sheet, Version 1, May 2020

KEYSIGHT TECHNOLOGIES

M8131A at a Glance

Key features

- 10 bit ADC
- 1, 2 or 4 channels, 6.5 GHz bandwidth (16 GSa/s)
- 1 or 2 channels, 12.5 GHz bandwidth (32 GSa/s)
- Spurious-free-dynamic range (SFDR) -66 dBc @ 1 GHz
- Harmonic distortion (HD) -67 dBc @ 1 GHz
- 8.0 effective number of bits (ENOB) @ 4 GHz (Option FDx)
- Internal clock oscillator or external 8 GHz clock or 10/100 MHz reference clock
- 2 GByte acquisition memory per module
- Form-factor: 2U AXIe module, controlled via external PC or AXIe system controller
- Part of Keysight's Wideband Solution Platform (WSP)

Optical data interface

- 4 x 160 Gb/s optical streaming interface
- Supports full rate, gapless streaming of raw or digitally down-converted samples into compatible storage, DSP or AWG devices or custom hardware
- Synchronization outputs for deterministic latency e.g. from the M8131A RF input to an AWG output

Choice of configurations

- Single ended inputs with adjustable sensitivity
  - 1, 2 or 4 channels, 4 GSa/s, 1.6 GHz useable bandwidth
  - 1, 2 or 4 channels, 16 GSa/s, 6.5 GHz bandwidth
  - 1 or 2 channels, 32 GSa/s, 12.5 GHz bandwidth
  - Adjustable input range: 40 mV_{pp} - 400 mV_{pp}
- Differential inputs with improved intrinsic noise and fixed input sensitivity
  - 1, 2 or 4 channels, 16 or 32 GSa/s, 12.5 GHz analog bandwidth
  - No antialiasing filter at the input allows operation in 2nd Nyquist band

Frequency Response correction

- Realtime digital frequency and phase response correction in with programmable coefficients – for frequency and phase response equalization of external devices in the input path, e.g. cables or amplifiers.

Digital down-conversion

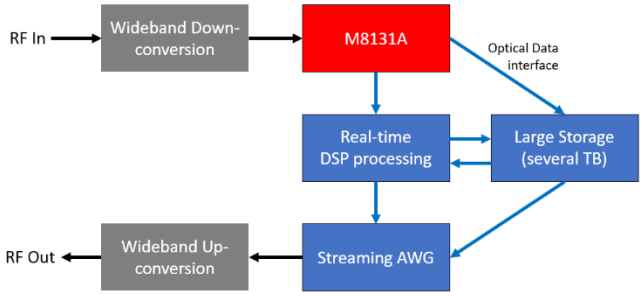
- Built-in digital down-conversion by powers of two from any IF frequency within the M8131A's bandwidth – simultaneously on all channels. The IF frequency can be set individually per channel.

Synchronization

- Synchronization of four M8131A modules (up to 16 channels @ 16 GSa/s or up to 8 channels @ 32 GSa/s) without additional hardware.

Wideband Solution Platform

The M8131A is part of Keysight's Wideband Solution Platform that consists of a portfolio of compatible instruments, including digitizer, arbitrary waveform generator, digital signal processor and storage modules. The interconnect between these products is based on a high-speed optical data interface.

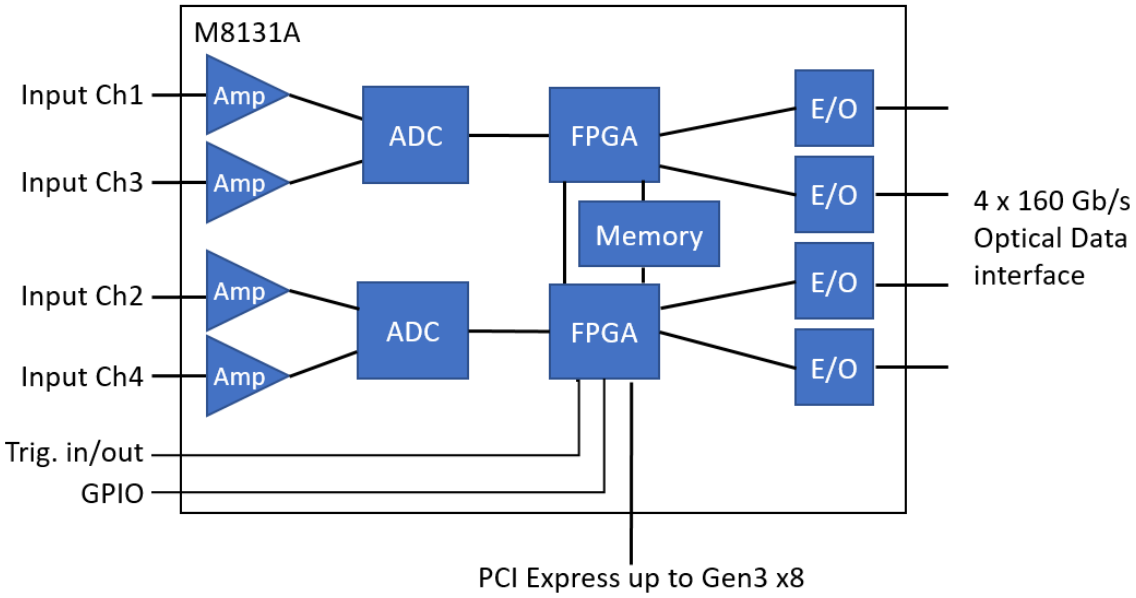


M8131A Overview

Conventional digitizers have a certain amount of built-in acquisition memory that allows the user to capture real-world signals for a certain, limited amount of time. Once the data has been captured, there is a dead-time during which the data is processed. But no matter how large the acquisition memory of a digitizer is, it is a finite resource and eventually data acquisition stops.

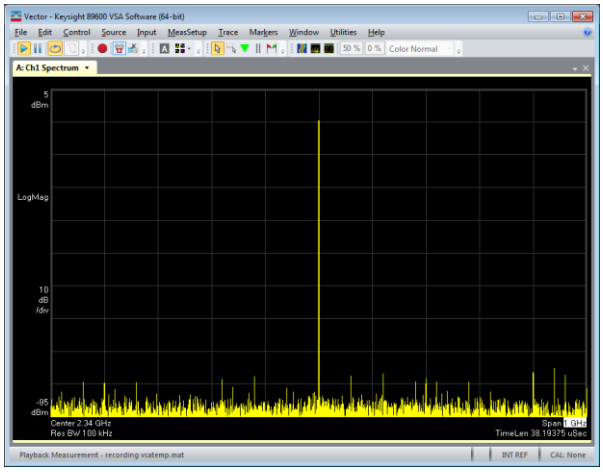
The M8131A offers – in addition to its build-in acquisition memory – an optical streaming interface (ODI), that allows gapless capture for an unlimited amount of time. Depending on the configuration, the M8131A can either stream the "raw" digitized samples or down-converted I/Q samples over the optical data interface.

The figure below shows an overview block diagram on the M8131A.



For full bandwidth streaming, the optical data interface must be used.

Wide bandwidth gapless streaming



The M8131A offers a unique combination of excellent signal fidelity, up to 12.5 GHz instantaneous bandwidth and gapless streaming at full bandwidth simultaneously.

In order to reduce the amount of (unnecessarily) captured data, a “segmented streaming” mode is also available. In this mode, data is only streamed when the IF magnitude is above a certain threshold. With the selection of fixed or variable size segment lengths, it is possible to achieve a 100% probability of intercept. In segmented streaming mode, each waveform segment is preceeded with a timestamp. This allows re-construction of the original signal.

Digital down-conversion

In addition to “direct mode”, where ADC samples are stored in internal memory or transmitted over the streaming interface, providing the full 6.5 GHz resp. 12.5 GHz of instantaneous bandwidth, the M8131A offers a “digital down-conversion” functionality for capturing lower bandwidth signals. In this mode, the digitized samples are multiplied with a (digital) local oscillator, low-pass filtered and decimated to a lower sample rate. Due to the lower sample rate, the resulting I/Q samples require less bandwidth and thus less storage for a given amount of capture time.

Another positive side effect of digital down-conversion is the processing gain: for every decimation by two, the signal-to-noise ratio (SNR) is improved by 3 dB or 0.5 bits of vertical resolution. As an example, if the required instantaneous bandwidth is only 800 MHz the digitized samples that were captured at 16 GSa/s can be decimated by a factor of 16 to 1 GSa/s. The corresponding SNR gain is log2(16) * 3 dB = 12 dB or 2 bits. In other words: for an 800 MHz wide input signal, the M8131A behaves like a 12-bit digitizer.

Optical Data Interface

The AXIe Consortium has standardized a high-speed optical data interface (ODI) for advanced instrumentation and embedded systems (http://www.axiestandard.org/odispecifications.html).

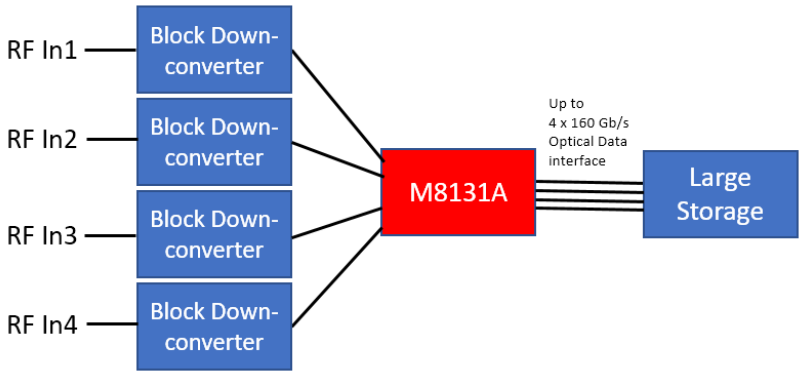
The M8131A has four ODI ports on the front panel, to transmit data at up to 160 Gb/s per port. Each of the optical interfaces has sufficient throughput to handle the data from one channel running at 16 GSa/s signal with 10 bits of resolution (= 160 Gb/s), In 32 GSa/s mode, two ODI interfaces are required to stream the captured data at full rate.

The optical data interface serves as a backbone between wideband digitizers, AWGs, digital signal processing modules, mass storage devices or custom hardware. Due to the modular structure, different system configurations can be realized. A few examples are shown in the following paragraphs.

Applications

Wideband gapless capture

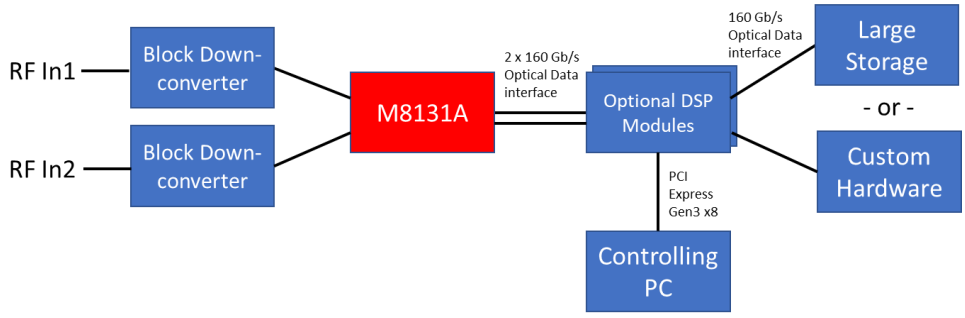
The M8131A together with a compatible mass storage device offers the unique capability to capture wideband scenarios without any gaps for minutes to hours to days – only limited by the capacity of the storage device. Up to 4 channels at 6.5 GHz bandwidth or 2 channels with up to 12.5 GHz bandwidth can be captured simultaneously using a single M8131A module. Combined with a compatible block down-converter **Error! Bookmark not defined.**, frequencies up to 44 GHz with modulation bandwidths up to 4 GHz can be covered.



Capture and process in real-time

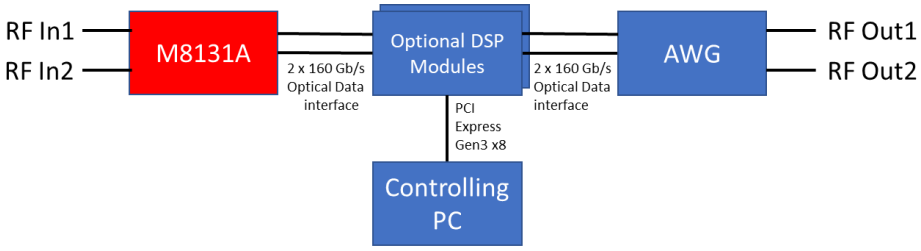
In many cases, the captured samples need to be post-processed in real-time. This can be accomplished in one of the two FPGA's inside the M8131A that is available for custom DSP functionality or in one or more compatible digital signal processing modules. Possible applications include:

- Demodulation of a communications signal
- Pulse-descriptor-word extraction from a received radar signal
- Real-time spectrum analysis
- Determination of the angle-of-arrival in a phased array antenna
- Custom digital signal processing



Record and playback

In combination with a compatible AWG, it is possible to put together a very wideband record and playback system. Depending on the amount of processing required, one or more digital signal processing modules can be inserted in the path.



Software

Since the M8131A is a faceless AXIe module, it requires a Soft Front Panel (SFP) application running on an external PC or AXIe embedded controller for operation. The SFP provides all the necessary controls to configure the M8131A acquisition system and streaming interface. It provides viewing areas to display the captured data in both time and frequency domain.

A SCPI interface is provided for applications to control the M8131A programmatically.

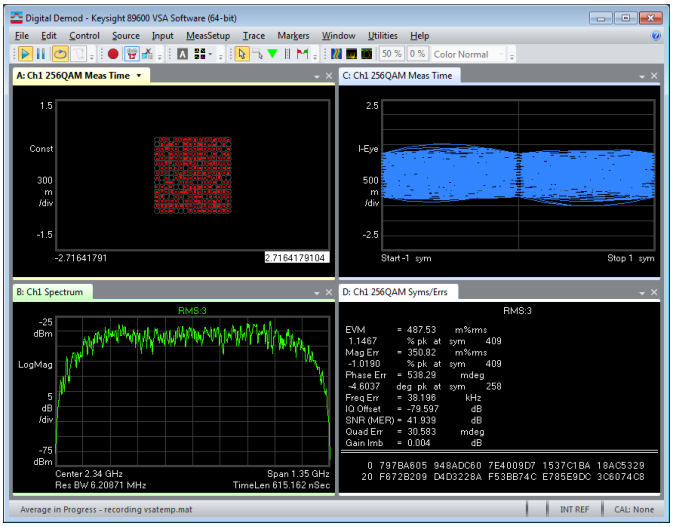
M8131A Soft Front Panel

VSA

For further analysis of captured data – particularly for frequency domain applications, the M8131A also works in conjunction with the Keysight 89600A Vector Signal Analysis (VSA) software.

The 89600A VSA software supports both the direct and digital down-conversion modes of the M8131A.

The 89600A VSA software is available.



VSA Software demodulating a captured QAM256 signal

Front Panel Connections

Options 011/012/014/061/062/064 modules have four single ended input connectors and four corresponding ODI connectors on the front panel.

A ‘Cal’ module connection is provided for the N2136A Digitizer calibration module.

Option 131/132 modules have two single ended input connectors. Corresponding to each input connector are two ODI connectors to handle the full rate of 32 GSa/s

A ‘Cal’ module connection is provided for the N2136A Digitizer calibration module.

Option FD1/FD2/FD4 modules have four pairs of differential input connectors and four corresponding ODI connector on the front panel.

All modules have a Sync In and four Sync Out connectors for synchronization with other M8131A modules, a Trigger In and Trigger Out connector, one sample clock input and two sample clock output as well as a Reference Clock Input and Output connectors.

In addition, all modules have a Control In/Out connector with 10 general purpose I/O signals as well as an FPGA Config connector which are reserved for future use.

Product Structure

The M8131A has a modular product structure and requires and AXIe chassis and an embedded AXIe controller or external PC to be operational. Also, the desired number of ODI cables (M8131A-831 / -833) must be ordered separately, depending on the number of ODI ports that will be used.

Description	Product #	Comment
1 channel, 4 GSa/s, 1.6 GHz bandwidth, single ended	M8131A-011	One of these options must be selected. Upgrade to higher channel count within the same bandwidth category is possible by software license (e.g. from 061 to 062). Upgrade from 1.6 GHz bandwidth to 6.5 GHz bandwidth is possible by software license (e.g. from 014 to 064).
2 channel, 4 GSa/s, 1.6 GHz bandwidth, single ended	M8131A-012	
4 channel, 4 GSa/s, 1.6 GHz bandwidth, single ended	M8131A-014	
1 channel, 16 GSa/s, 6.5 GHz bandwidth, single ended	M8131A-061	
2 channel, 16 GSa/s, 6.5 GHz bandwidth, single ended	M8131A-062	
4 channel, 16 GSa/s, 6.5 GHz bandwidth, single ended	M8131A-064	
1 channel, 32 GSa/s, 12.5 GHz bandwidth, single ended	M8131A-131	
2 channel, 32 GSa/s, 12.5 GHz bandwidth, single ended	M8131A-132	
1 channel, 16 GSa/s, differential input	M8131A-FD1	
2 channel, 16 GSa/s or 1 channel, 32 GSa/s, diff. input	M8131A-FD2	
4 channel, 16 GSa/s or 2 channel, 32 GSa/s, diff. input	M8131A-FD4	
Streaming via optical data interface	M8131A-STR	Optional software licenses
Digital Down-conversion	M8131A-DDC	
Segmented Streaming	M8131A-SEG	
ISO 17025 Report	M8131A-1A7	
Z540 Calibration Report	M8131A-Z54	
Bundle with M9502A 2-slot AXIe chassis	M8131A-BU2	Optional (if none is selected, an AXIe chassis must be purchased separately)
Bundle with M9505A 5-slot AXIe chassis	M8131A-BU5	
Bundle with M9505A 5-slot AXIe chassis and embedded controller	M8131A-BU6	

Accessories

Description	Product #	Comment
Microwave phase matched balun, 20 GHz, SMA jack	M8131A-801	Recommended for differential input channels (Opt. FDx) to improve second harmonics
Cable assembly coaxial–50 Ω, SMA to SMA, 457 mm	M8131A-810	
Cable assembly coaxial–50 Ω, SMA to SMA, 1220 mm	M8131A-811	
Connector-RF, SMA termination, plug straight, 50 Ω, 12.4 GHz, 0.5 W	M8131A-820	Recommended for differential input channels (Opt. FDx) used in single ended mode
Optical Data Interface cable, 1 m	M8131A-831	No ODI cables are included. Please order the desired number of cables separately
Optical Data Interface cable, 3 m	M8131A-833	

Additional RF sample clock jumper cable	M8131-61610	Sample Clk Out to Sample Clk In semi-rigid cable
Digitizer Calibration Module for M8131A, 2.92 mm	N2136A	Recommended with options 01x, 06x, 13x

Upgrades

Description	Product #	Comment
Upgrade from 1.6 GHz to 6.5 GHz, 1 channel	M8131AU-U61	
Upgrade from 1.6 GHz to 6.5 GHz, 2 channel	M8131AU-U62	
Upgrade from 1.6 GHz to 6.5 GHz, 4 channel	M8131AU-U64	
Upgrade 4 GSa/s, 1.6 GHz Digitzer to from 1 to 2 channels	M8131AU-012	Upgrade from 1 to 4 ch. requires 012 and 014
Upgrade 4 GSa/s, 1.6 GHz Digitzer to from 2 to 4 channels	M8131AU-014	
Upgrade 16 GSa/s, 6.5 GHz Digitizer from 1 to 2 channels	M8131AU-062	Upgrade from 1 to 4 ch. requires 062 and 064
Upgrade 16 GSa/s, 6.5 GHz Digitizer from 2 to 4 channels	M8131AU-064	
Upgrade 32 GSa/s, 12.5 GHz Digitizer from 1 to 2 channels	M8131AU-132	
Upgrade 16/32 GSa/s Digitizer from 1 to 2 channels	M8131AU-FD2	Upgrade from 1 to 4 ch. requires FD2 and FD4
Upgrade 16/32 GSa/s Digitizer from 2 to 4 channels	M8131AU-FD4	
Streaming via optical data interface	M8131AU-STR	
Digital Down-conversion	M8131AU-DDC	
Segmented Streaming	M8131AU-SEG	Available with SW Rev. 4

AXIe

The M8131A is a modular instrument packaged in the AXIe form factor. AXIe is a new open standard for high-performance, modular instrumentation, and incorporates the best features of other modular formats including VXIbus, LXI and PXI. Keysight offers a line of scalable chassis in this powerful format.

Two form factors are available: two-slot and five-slot chassis. These include an embedded AXIe system module that does not occupy a module slot. In addition, an AXIe embedded controller is an entire system that can control the digitizer. This controller consumes one module slot in the chassis. The chassis can be used on the bench or in a rack, occupying only 4U of rack space.

Description	Product #	Comment
2-slot AXIe chassis with USB option	M9502A-U20	
5-slot AXIe chassis with USB option	M9505A-U20	
5-slot AXIe chassis with Thunderbolt	M9506A	
PCIe desktop card adapter x8 Gen 2 / Gen 3	M9048A / B	
PCIe desktop card adapter dual port x16 Gen 3	M9049A	
x8 – x8 PCIe cable	Y1202A	
Embedded AXIe controller	M9537A	

Performance Characteristics

Analog inputs

	Option FDx	Option 01x, 06x	Option 13x
Number of channels	1, 2 or 4	1, 2 or 4	1 or 2
Analog bandwidth (3 dB)	12.5 GHz (typ.)	6.5 GHz (typ.)	12.5 GHz (typ.)
Sample rate	4 ch @16 GSa/s or 2 ch @ 32 GSa/s, selectable by software	Opt. 06x: 16 GSa/s Opt 01x: 16 GSa/s, decimated by 4	32 GSa/s
Rise/fall time 20 to 80% (calculated as 0.31/BW)	25 ps (typ.)	Opt 06x: 48 ps (typ.) Opt 01x: 196 ps (typ.)	25 ps (typ.)
Vertical Resolution	10 bits	10 bits	
Input type	Differential	Single-ended	
Input impedance	100 Ω ± 3.5% (typ.)	50 Ω ± 3.5% (typ.)	
Input sensitivity	62.5 mV/div	5, 10, 20, 50 mV/div	
Full scale range	500 mV	40 mV, 80 mV, 160 mV, 400 mV	
Input coupling	DC	DC	
Channel-to-channel isolation (all values are typical)	16 GSa/s: -70 dBc, f_{in} = DC…1 GHz -52 dBc, f_{in} = 1…5 GHz 32 GSa/s: -70 dBc, f_{in} = DC…1 GHz -62 dBc, f_{in} = 1…5 GHz	-70 dBc, f_{in}=DC…1 GHz -52 dBc, fin = 1…3 GHz -45 dBc, fin = 3…5 GHz	-70 dBc, f_{in}=DC…1 GHz -52 dBc, f_{in} = 1…3 GHz -45 dBc, fin = 3…5 GHz
DC gain accuracy	n/a	± 3% (typ.)	
Offset range	0 V (typ.), fix	-400 mV to +400 mV	
Offset resolution	n/a	100 µV (nom.)	
Offset accuracy	± (2.5% + 10 mV) (typ.)	± (2.5% + 10 mV) (typ.)	
Differential offset	0 mV ± 10 mV (typ.)	n/a	
Skew between normal and complement	0 ps ± 1 ps (nom.)	n/a	
Skew between any pair of inputs	0 ps ± 5 ps (nom.)	0 ps ± 5 ps (nom.)	
Connector type	3.5 mm (f)		

<table>
<tr><th></th><th>Option FDx</th><th>Option 01x, 06x</th><th>Option 13x</th></tr>
<tr><td>ENOB @ -6 dBFS
(all values are typical) [1,2]</td><td>16 GSa/s
9.3, bw: DC…0.5 GHz
8.3, bw: DC…2.0 GHz
7.8, bw: DC…4.0 GHz
7.4, bw: DC…6.5 GHz

32 GSa/s
9.6, bw: DC…0.5 GHz
8.6, bw: DC…2.0 GHz
8.3, bw: DC…4.0 GHz
7.6, bw: DC…8.0 GHz
6.6, bw: DC…12.5 GHz</td><td>Input range 400 mV_{pp}
(Option 06x)
8.3, bw: DC…0.5 GHz
7.8, bw: DC…2.0 GHz
7.4, bw: DC…4.0 GHz
7.0, bw: DC…6.5 GHz

Input range 400 mV_{pp}
(Option 01x)
7.0, bw: DC…2.0 GHz</td><td>Input range 400 mV_{pp}
8.3, bw: DC…0.5 GHz
8.0, bw: DC…2.0 GHz
7.7, bw: DC…4.0 GHz
7.2, bw: DC…8.0 GHz
6.4, bw: DC…12.5 GHz</td></tr>
<tr><td>RMS noise floor
(all values are typical) [1,2]</td><td>16 GSa/s
<table><tr><td>Input sensitivity</td><td>V_{RMS}</td></tr><tr><td>62.5 mV / div</td><td>780 µV</td></tr></table>
32 GSa/s
<table><tr><td>Input sensitivity</td><td>V_{RMS}</td></tr><tr><td>62.5 mV / div</td><td>780 µV</td></tr></table></td><td><table><tr><td>Input sensitivity</td><td>V_{RMS}</td></tr><tr><td>5 mV / div</td><td>180 µV</td></tr><tr><td>10 mV / div</td><td>240 µV</td></tr><tr><td>20 mV / div</td><td>360 µV</td></tr><tr><td>50 mV / div</td><td>780 µV</td></tr></table></td><td><table><tr><td>Input sensitivity</td><td>V_{RMS}</td></tr><tr><td>5 mV / div</td><td>180 µV</td></tr><tr><td>10 mV / div</td><td>240 µV</td></tr><tr><td>20 mV / div</td><td>360 µV</td></tr><tr><td>50 mV / div</td><td>780 µV</td></tr></table></td></tr>
<tr><td>Amplitude flatness
(all values are typical)</td><td>16 GSa/s
± 0.2 dB, f_{in}= DC…2.0 GHz
± 0.7 dB, f_{in}= 2.0…6.0 GHz

32 GSa/s
± 0.2 dB, f_{in}= DC…2.0 GHz
± 0.7 dB, f_{in}= 2.0…6.0 GHz
± 0.9 dB, f_{in}= 6.0…9.0 GHz
± 1.6 dB, f_{in}= 9.0…12 GHz</td><td>± 0.2 dB, f_{in}= DC…6 GHz
± 0.3 dB, f_{in}= 2.0…6 GHz</td><td>± 0.2 dB, f_{in}= DC…2.0 GHz
± 0.3 dB, f_{in}= 2.0…6.0 GHz
± 0.7 dB, f_{in} = 6.0...9.0 GHz [1]
± 0.9 dB, f_{in} = 9.0...12 GHz [1]</td></tr>
</table>

[1] Specifications are valid within ± 10 K temperature change and within 8 GHz ± 10 ppm sample clock frequency referenced to last calibration conditions.
[2] M8131A-FDx measured with a balun (e.g. HL 9402).

2nd Harmonic @ -1 dBFS (all values are typical) [1,2]	*16 GSa/s* -67 dBc, f_{in} = DC…1 GHz -63 dBc, f_{in} = 1…2 GHz -59 dBc, f_{in} = 2…3 GHz *32 GSa/s* -67 dBc, f_{in} = DC…1 GHz -63 dBc, f_{in} = 1…2 GHz -58 dBc, f_{in} = 2…4 GHz -50 dBc, f_{in} = 4…6 GHz	*Input range* 400 mV_{pp} -55 dBc, f_{in} =DC…2 GHz -54 dBc, f_{in} = 2…3 GHz	*Input range* 400 mV_{pp} -54 dBc, f_{in} = DC…2 GHz -52 dBc, f_{in} = 2…4 GHz -50 dBc, f_{in} = 4…6 GHz
3rd Harmonic @ -1 dBFS (all values are typical) [1,2]	*16 GSa/s* -60 dBc, f_{in} = DC…1 GHz -56 dBc, f_{in} = 1…2 GHz *32 GSa/s* -58 dBc, f_{in}= DC…1 GHz -54 dBc, f_{in}= 1…2 GHz -49 dBc, f_{in}= 2…4 GHz	*Input range 400 mV_{pp}* -50 dBc, f_{in} = DC…1 GHz -47 dBc, f_{in} = 1…2 GHz	*Input range 400 mV_{pp}* -50 dBc, f_{in}= DC…1 GHz -47 dBc, f_{in}=1…2 GHz -45 dBc, f_{in}=2…4 GHz
SFDR @ -1 dBFS (excluding harmonic distortion) (all values are typical) [1,2]	*16 GSa/s* -66 dBc, f_{in} = DC…1 GHz, -63 dBc, f_{in} = 1…3 GHz, -55 dBc, f_{in} = 3…6 GHz, all measured DC to 6 GHz band *32 GSa/s* -51 dBc, f_{in} = DC…3 GHz, -50 dBc, f_{in} = 3…5 GHz, -46 dBc, f_{in} = 5…7 GHz, -42 dBc, f_{in} = 7…9 GHz, -38 dBc, f_{in} = 9…12 GHz, all measured DC to 12 GHz band	*Input range 400 mV_{pp}* -58 dBc, f_{in}= DC…1 GHz, -55 dBc, f_{in}= 1…3 GHz, -53 dBc, f_{in}= 3…6 GHz, all measured DC to 6 GHz band	*Input range 400 mV_{pp}* -51 dBc, f_{in}= DC…3 GHz, -50 dBc, f_{in}= 3…5 GHz, -46 dBc, f_{in}= 5…7 GHz, -40 dBc, f_{in}= 7…9 GHz, -38 dBc, f_{in}= 9…12 GHz, all measured DC to 12 GHz band

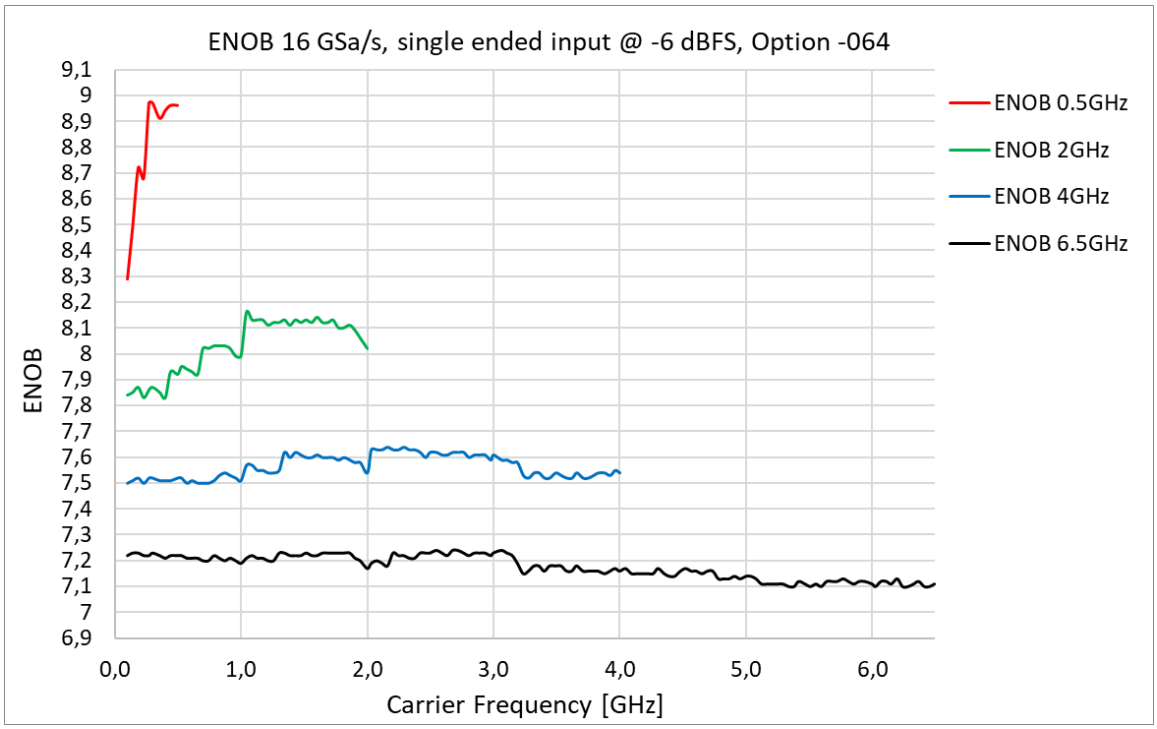
SFDR @ -1 dBFS (excluding harmonic distortion) (all values are typical) [1,2] In-band	*16 GSa/s* -65 dBc, f_{in} = DC…3 GHz, measured DC to 3 GHz band -57 dBc, f_{in} = 3…6 GHz, measured 3 to 6 GHz band *32 GSa/s* -63 dBc, f_{in} = DC…4 GHz, measured DC to 4 GHz band -55 dBc, f_{in} = 4…8 GHz, measured 4 to 8 GHz band -52 dBc, f_{in} = 8…12 GHz, measured 8 to 12 GHz band	*Input range 400 mV_{pp}* --65 dBc, f_{in} = DC…3GHz, measured DC to 3 GHz band -57 dBc, f_{in} = 3…6 GHz, measured 3 to 6 GHz band	*Input range 400 mV_{pp}* 63 dBc, f_{in} = DC…4 GHz, measured DC to 4 GHz band -55 dBc, f_{in} = 4…8 GHz, measured 4 to 8 GHz band -52 dBc, f_{in} = 8…12 GHz, measured 8 to 12 GHz band

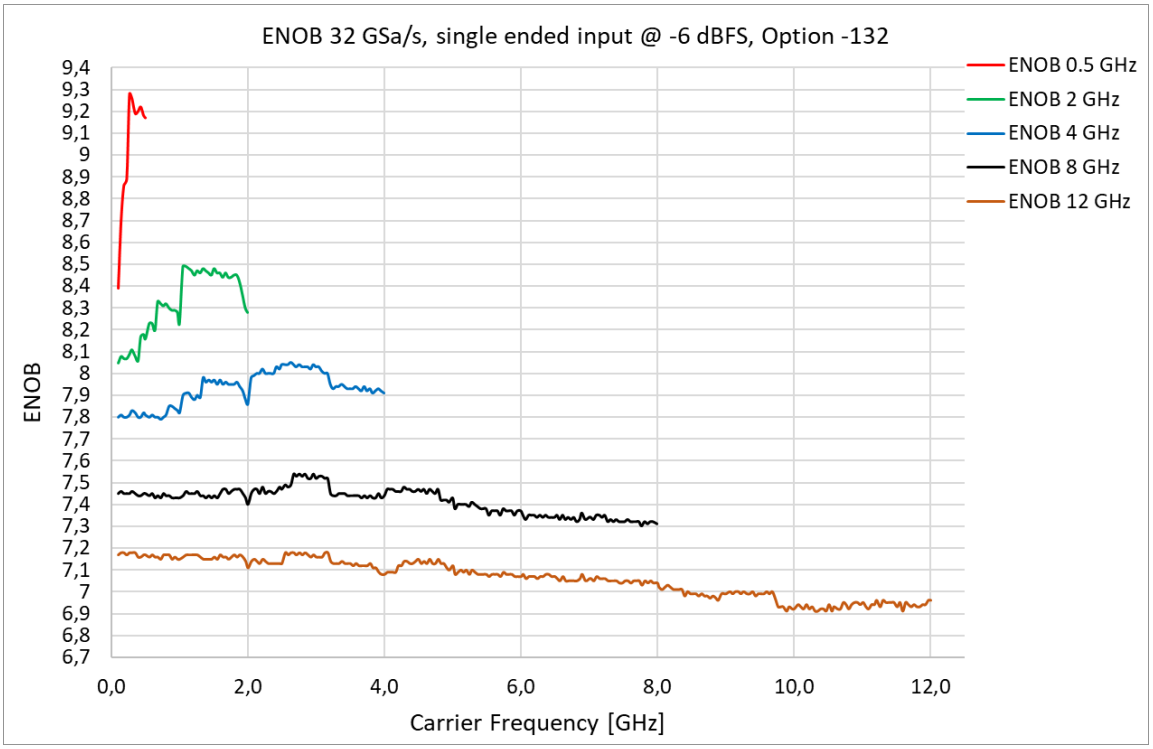
Phase noise

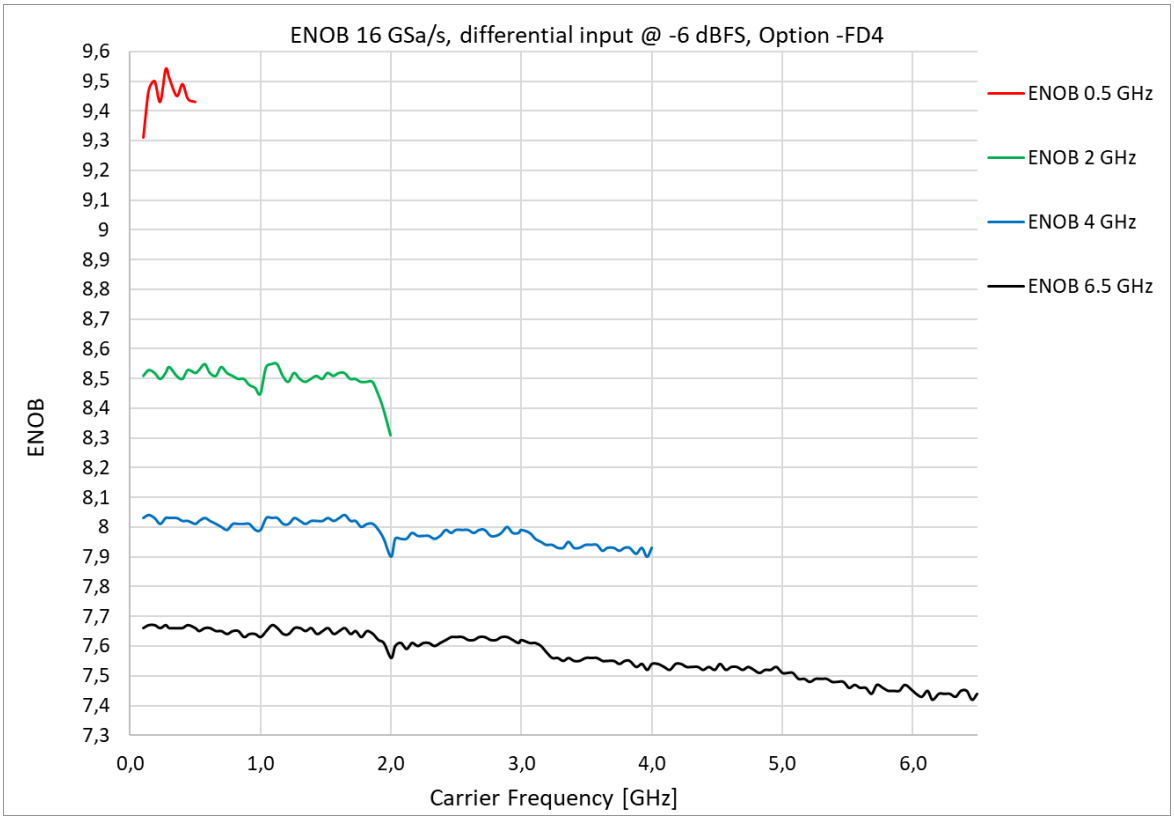
The following plot shows the measured phase noise of the internal sample clock.

ENOB vs. frequency

The following plot shows ENOB measured versus frequency of the M8131A with different input options using -6 dBFS input levels. The ENOB values are calculated according to IEEE 1241-2000. Bandwidth is limited to the maximum tone frequency.






ENOB 16 GSa/s, differential input @ -6 dBFS, Option -FD4
ENOB
Carrier Frequency [GHz]
ENOB 0.5 GHz
ENOB 2 GHz
ENOB 4 GHz
ENOB 6.5 GHz
9,6
9,5
9,4
9,3
9,2
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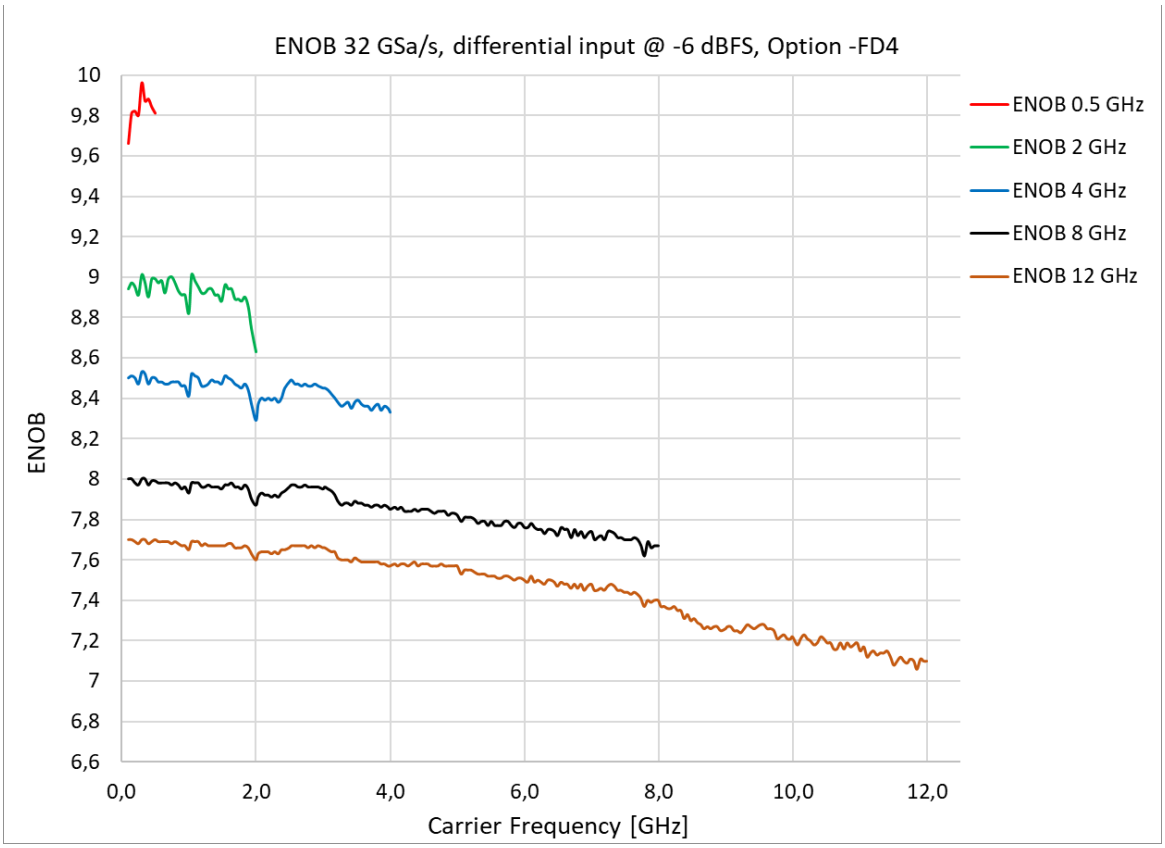
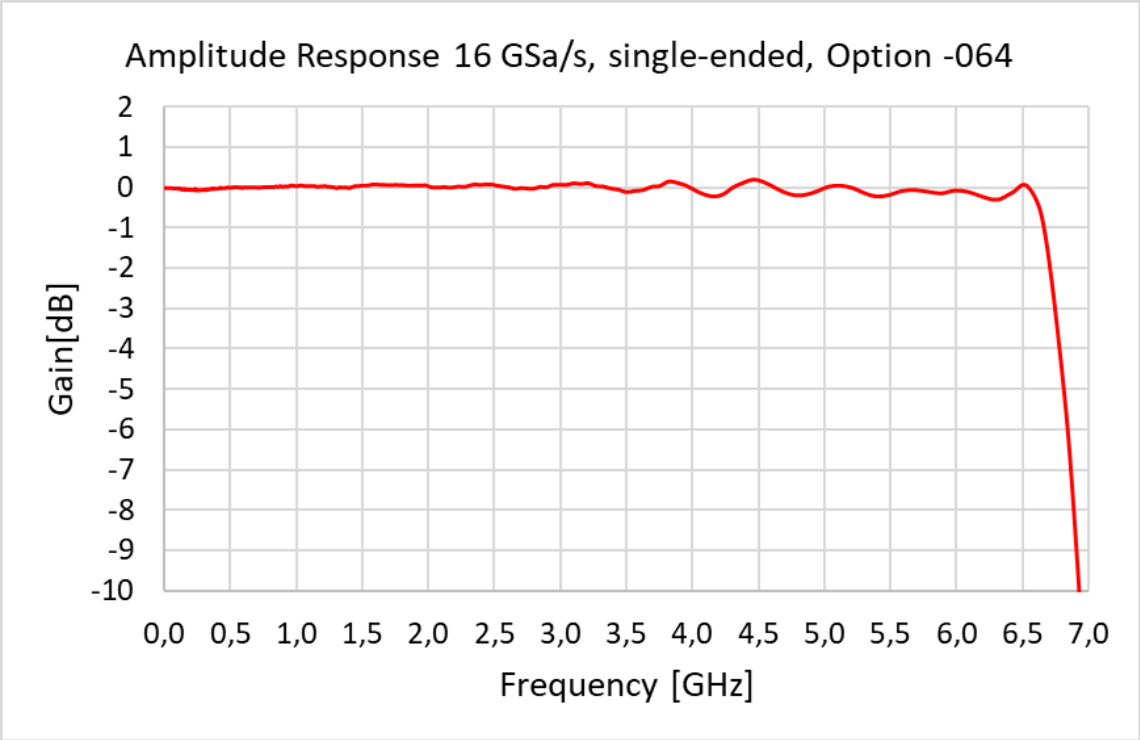
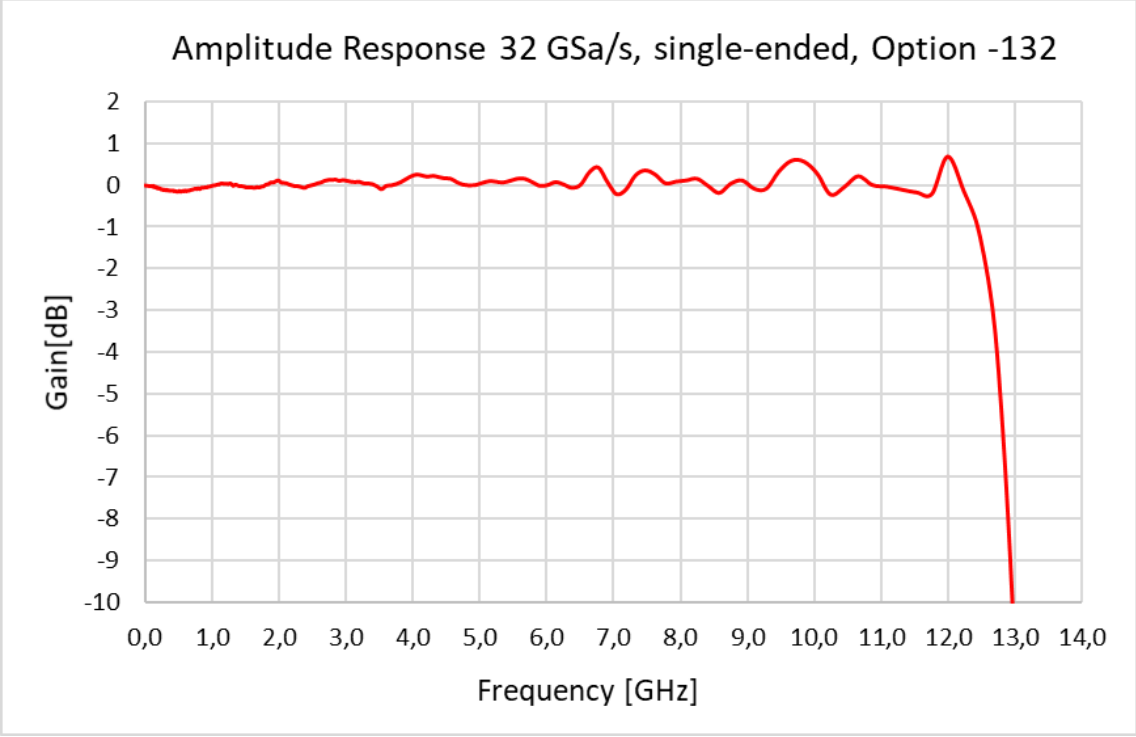
5,0
6,0

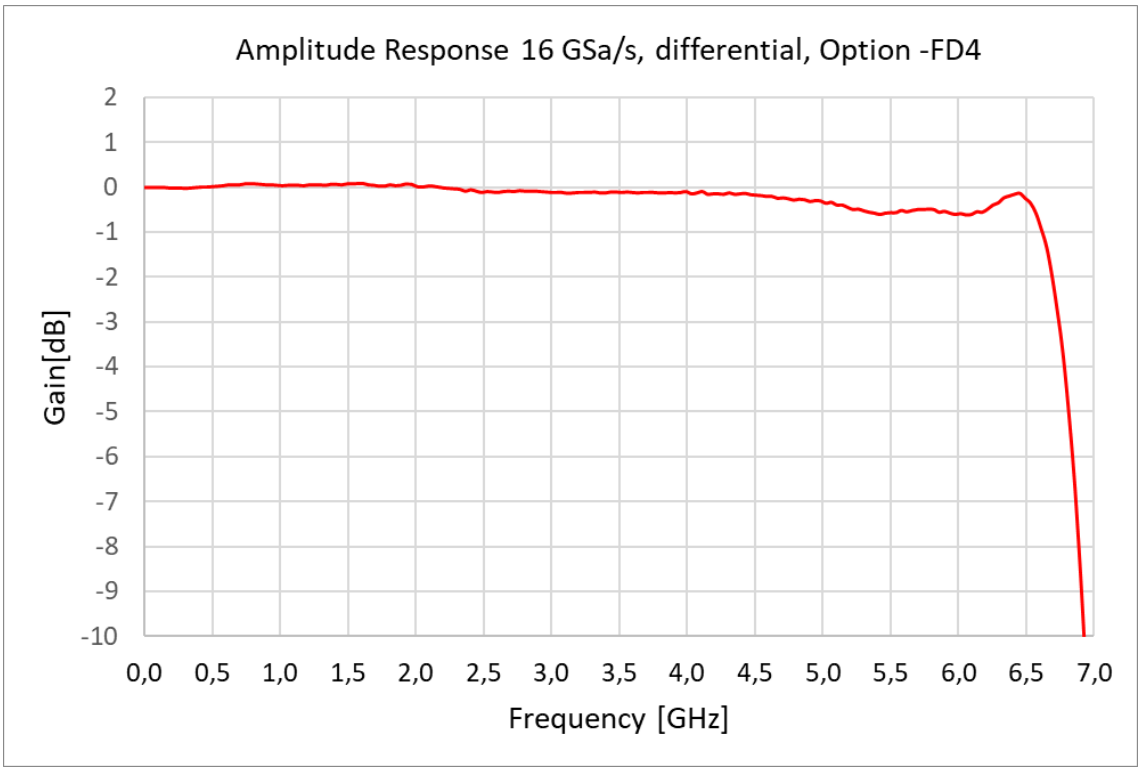

ENOB 32 GSa/s, differential input @ -6 dBFS, Option -FD4
ENOB
Carrier Frequency [GHz]
ENOB 0.5 GHz
ENOB 2 GHz
ENOB 4 GHz
ENOB 8 GHz
ENOB 12 GHz
10
9,8
9,6
9,4
9,2
9
8,8
8,6
8,4
8,2
8
7,8
7,6
7,4
7,2
7
6,8
6,6
0,0
2,0
4,0
6,0
8,0
10,0
12,0

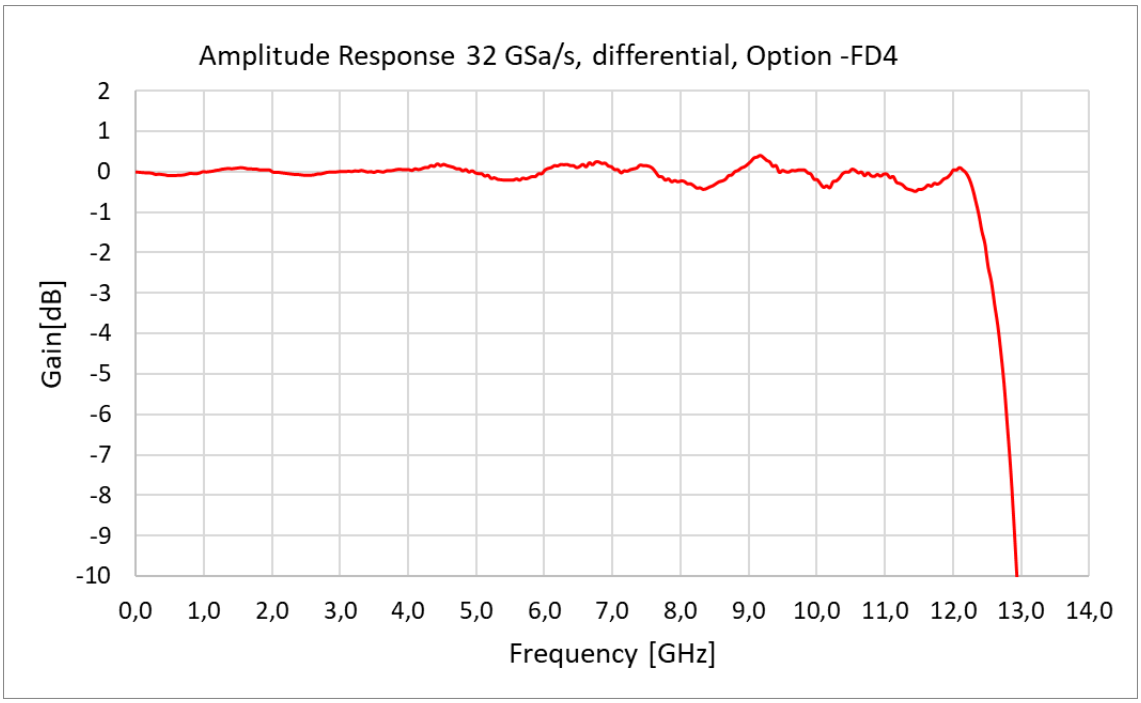
Amplitude response measurements

Following graphs show measurements of the amplitude response of the different M8131A input options 064 @ 16 GSa/s, 132 @ 32 GSa/s, FD4 @ 16 GSa/s, FD4 @ 32 GSa/s.



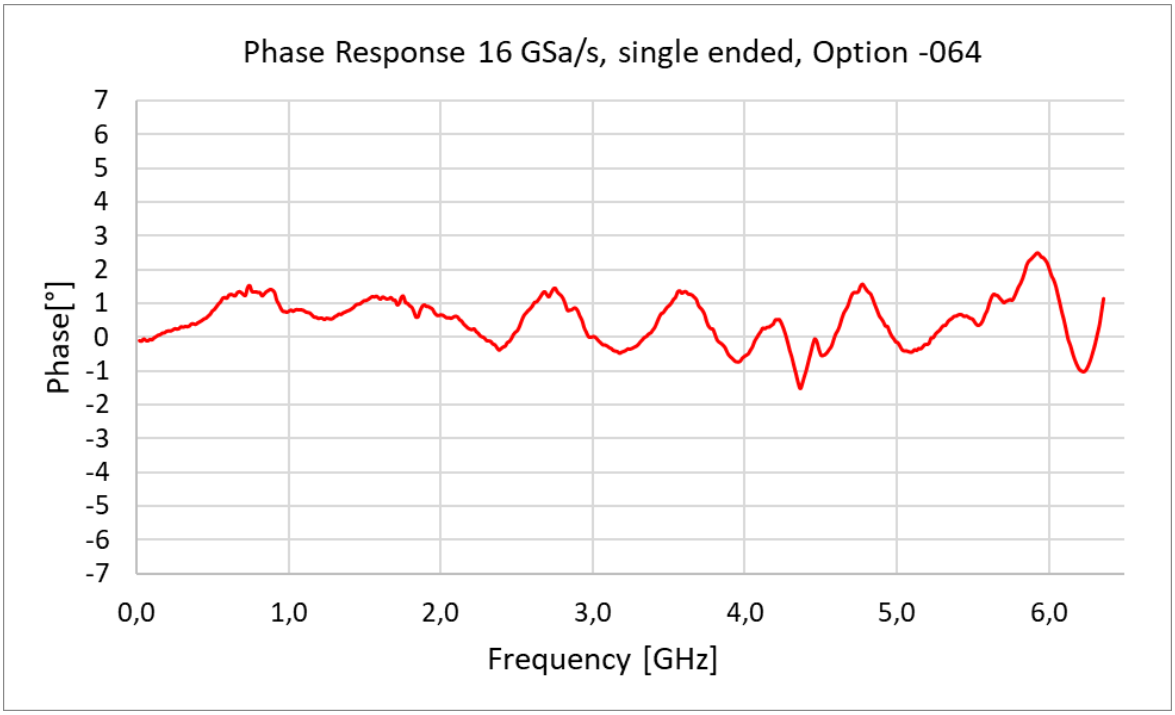


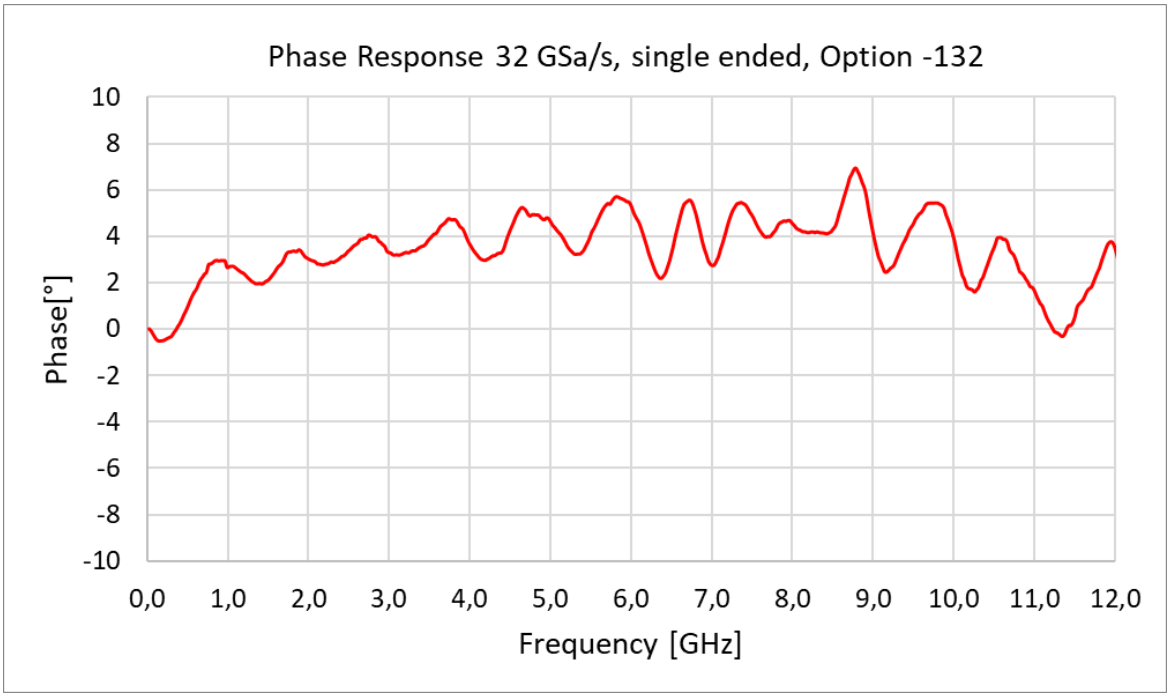

Amplitude Response 16 GSa/s, differential, Option -FD4
Gain[dB]
2
1
0
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
0,0 0,5 1,0 1,5 2,0 2,5 3,0 3,5 4,0 4,5 5,0 5,5 6,0 6,5 7,0
Frequency [GHz]

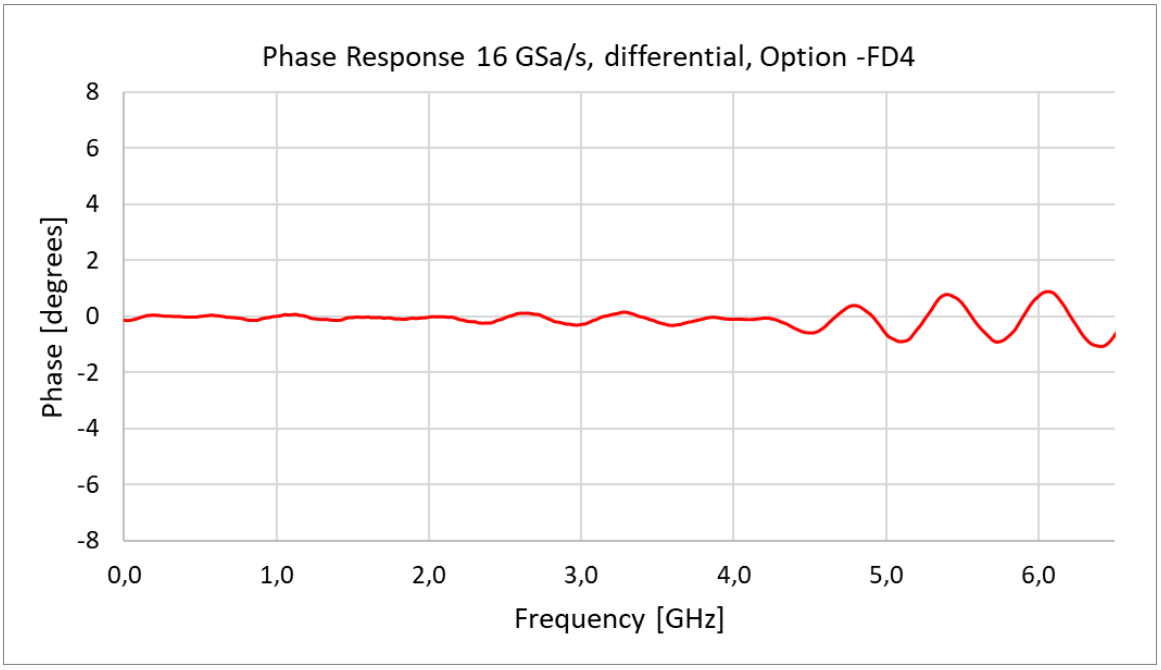

Amplitude Response 32 GSa/s, differential, Option -FD4
Gain[dB]
2
1
0
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
0,0 1,0 2,0 3,0 4,0 5,0 6,0 7,0 8,0 9,0 10,0 11,0 12,0 13,0 14,0
Frequency [GHz]

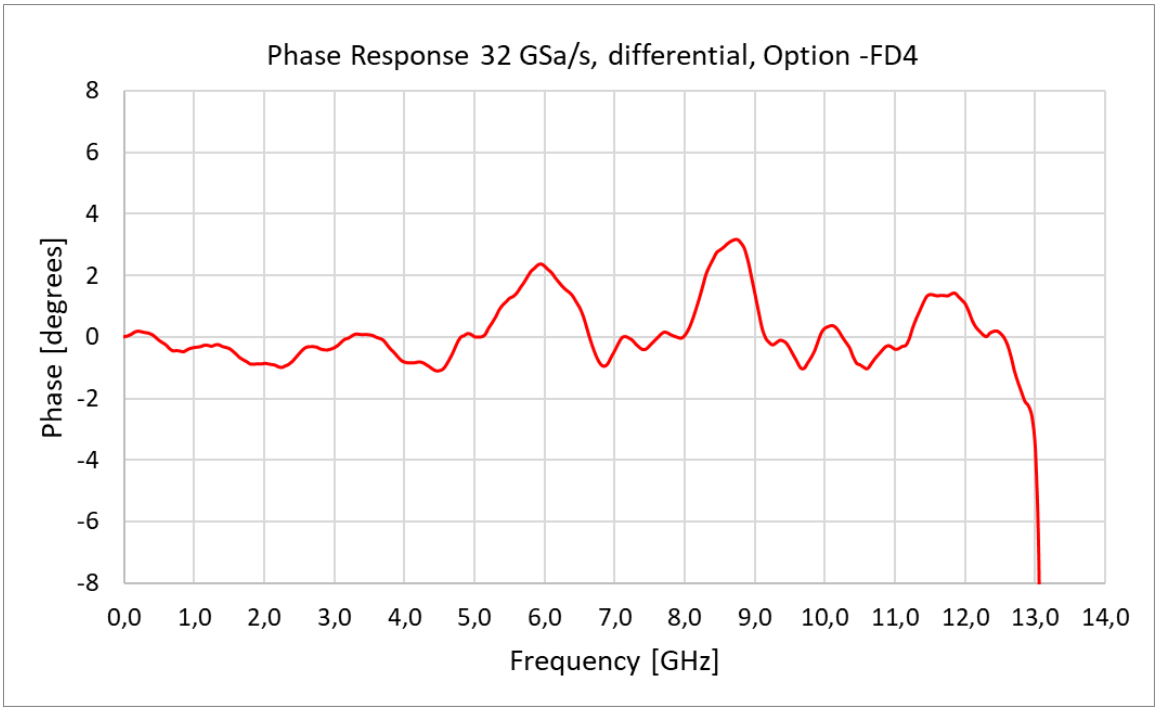
Phase response measurements

Following graphs show measurements of the phase response of the different M8131A input options 064 @ 16 GSa/s, 132 @ 32 GSa/s, FD4 @ 16 GSa/s, FD4 @ 32 GSa/s.






Phase Response 16 GSa/s, differential, Option -FD4
Phase [degrees]
8
6
4
2
0
-2
-4
-6
-8
0,0
1,0
2,0
3,0
4,0
5,0
6,0
Frequency [GHz]


Phase Response 32 GSa/s, differential, Option -FD4
Phase [degrees]
8
6
4
2
0
-2
-4
-6
-8
0,0
1,0
2,0
3,0
4,0
5,0
6,0
7,0
8,0
9,0
10,0
11,0
12,0
13,0
14,0
Frequency [GHz]

Trigger In

A trigger input is provided at the front-panel of the M8131A module.

The LED next to the Trigger In connector indicates that an externally applied signal matches the adjusted threshold to be used as a Trigger event.

Input range	-2 to +2 V
Threshold	
Range	-2 to +2 V
Resolution	10 mV (nom.)
Sensitivity	100 mV (typ.)
Polarity	Selectable: positive or negative
Drive	Always all channels
Input impedance	50 Ω (nom.), DC coupled
Connector	SMA

Trigger Out

A Trigger Output is provided at the front panel of the M8131A module. An internally generated Trigger Event generates a pulse at Trigger Out.

Output voltage	
High Level	1.1 V (typ.), terminate externally with 50 Ω to GND
Low Level	0.35 V (typ.), terminate externally with 50 Ω to GND
Rise / fall time (20% / 80 %)	70 ps (nom.)
Pulse width	100 ns (nom.)
Output impedance	50 Ω (nom.)
Connector	SMA

Timing Characteristics

Analog Input to Trigger Out	170 ns (meas.)
Analog Input to ODI Out	540 ns (meas.), DDC = Off, Decimation = 1 640 ns (meas.), DDC = Off, Decimation = 2, 4 750 ns (meas.), DDC = On, Decimation = 4, 8, …512

Trigger Events

A trigger can be caused by one of the following events:

Hardware Trigger	Active edge on the Trigger Input on the Front Panel
Trigger on Waveform Rising edge, voltage level Falling edge, voltage level	A trigger event is generated based on a condition of the signal captured on one of the analog channels. Only available in Direct Mode (DDC = Off)
Trigger on IF Magnitude Rising edge, power level Falling edge, power level	A trigger event is generated based on the power level of the digitally down-converted power level. Only available in DDC mode.

Time stamp timing accuracy in segmented mode	50 fs $_{RMS}$ (meas.)

Mode	Trigger Source	Min. Trigger Pulse Width (all values are nom.)	Min. Trigger Inactive Time (all values are nom.)
Direct (DDC = Off)	Hardware Trigger Trigger on Waveform	5 ns 62.5 ps	5 ns 5 ns
DDC 16 GSa/s (DDC = On)	Hardware Trigger Trigger on IF Magnitude	5 ns 62.5 ps * decimation factor	2 ns * decimation factor 2 ns * decimation factor
DDC 32 Sa/s (DDC = On)	Hardware Trigger Trigger on IF Magnitude	5 ns 31.25 ps * decimation factor	2 ns * decimation factor 2 ns * decimation factor

Reference Clock Input

A reference clock input is provided on the front panel of the M8131A module.

Input frequency	Selectable: 10 MHz or 100 MHz
Lock range	± 20 ppm (typ.)
Input level	632 mV_{pp} (0 dBm) to 3.1 V_{pp} (14 dBm) (typ.)
Input impedance	50 Ω (nom.), AC coupled
Connector Type	3.5 mm (f)

Reference Clock Output

A reference clock output is provided on the front panel of the M8131A module.

Reference Clock Source: Internal Reference Clock Oscillator	
Output frequency	100 MHz
Frequency accuracy	± 0.5 ppm initial accuracy (spec.) aging less than 1 ppm in 15 years (typ.)
Phase Noise	< -143 dBc/Hz (meas.) at 10 kHz offset, f_{OUT} = 100 MHz
Output Power	8 dBm ± 2 dB (typ.)

Reference Clock Source: External Reference Clock Input	
Output frequency	100 MHz
Frequency accuracy	Same as applied at Reference Clock Input
Phase Noise	Determined by phase noise at Reference Clock Input
Output Power	
10 MHz reference clock input	8 dBm ± 2 dB (typ.)
100 MHz reference clock input	8 dBm ± 2 dB (typ.)

Source impedance	50 Ω (nom.), AC coupled
Connector type	3.5 mm (f)

Sample Clock Input

A sample clock input is provided on the front panel of the M8131A module. It is used as the sample clock for all four channels of the M8131A. A sample clock input signal must always be provided – either through a loop-back connection to the sample clock out or by an external signal generator

Input frequency	8 GHz
Frequency accuracy	± 20 ppm (typ.)
Input Power	+2 dBm to +10 dBm (typ.)
Impedance	50 Ω (nom.), AC coupled
Connector Type	SMA

Sample Clock Output

Two identical 8 GHz Sample Clock Outputs are provided at the front panel of the M8131A. One Sample Clock Output can be used to drive the Sample Clock Input of the same M8131A. A semi-rigid loopback cable is provided with the M8131A to connect the Sample Clock Output connector with the Sample Clock Input connector. The second Sample Clock Output can be used to drive a second M8131A or an AWG for phase coherent operation.

Number of sample clock outputs	2 - unused sample clock outputs must be terminated with 50 Ω
Output frequency	8 GHz
Source: internal synthesizer	
Frequency accuracy	± 0.5 ppm initial accuracy (spec.) aging less than 1 ppm in 15 years (typ.)
Phase noise	< -105 dBc/Hz (typ.) at 10 kHz offset, f_{OUT} = 8 GHz
Output power	8 dBm ± 2.5 dB (typ.)
Source impedance	50 Ω, AC coupled (nom.)
Connector type	3.5 mm (f)

Optical Data Interface

The Optical Data Interface (ODI) is a high-speed interface standard for advanced instrumentation from the AXIe Consortium. Documentation of the ODI specification can be found at: www.axiestandard.org/odispecifications.html.

ODI Physical Interface characteristics

Specification	ODI-1: Physical Layer Specification, Revision 3.0
Number of physical ODI ports	Four physical ODI ports • One ODI port per ADC channel at 16 GSa/s, • Two ODI ports per ADC channel at 32 GSa/s
Connector	MPO style, 2 rows of 12 fiber positions
Lane rate	14.1 Gbit/s
Interlaken Burst Max	Selectable: 256 or 2048
Flow control	None
Port Directionality	Producer only (Bi-directional for self test purposes)
Port Aggregation	16 GSa/s: Not applicable 32 GSa/s: 2 physical ODI ports
Interlaken Channels	1 channel (Ch 0)
Streaming Data Rate	20 GByte/s (160 Gbit/s) maximum per physical ODI port

ODI Data Format capability

Specification	ODI-2: Transport Layer, Revision 3.0, ODI-2.1: High Speed Data Formats, Revision 3.0
Packet Types supported	NO_HEADER, VITA49_IF_DATA
Context packets	Not used
Control packets	Not used
Timestamp support	UTC
Trailer bit support	None
Signal Data Packet Size	32000 bytes, fix

Supported Data Formats

Item Packing Field Width	Data Item (signed)	Event bits	Real or IQ	Channels	Notes
16	16 bit	0	Real	1	Used in direct mode with decimation factor ≥ 2
10	10 bit	0	Real	1	Used in direct mode at full sample rate with no decimation
16	16 bit	0	IQ	1	Used in digital down-conversion mode

Control Input/Output

A bidirectional parallel port with 10 digital I/O signals is provided on the front panel. This functionality is reserved for future use.

FPGA Config Connector

This connector is reserved for future use.

Digital down-conversion

Digital down-conversion (DDC) is achieved by complex multiplication with an (digital) local oscillator, which results in complex-valued IQ samples. Decimation is achieved by digital filtering, which suppresses unwanted aliases. In DDC mode, data is always captured down-converted and decimated as 16-bit I and 16-bit Q data.

The selection of DDC vs. direct mode and the decimation factor applies to all channels of a module. However, the LO frequency can be chosen individually per channel.

Decimation factors	4, 8, 16, 32, 64, 128, 256, 512
LO frequency	
Range	-6.5 GHz to +6.5 GHz in 16 GSa/s mode -12.5 GHz to +12.5 GHz in 32 GSa/s mode
Resolution	57 µHz in 16 GSa/s mode 114 µHz in 32 GSa/s mode
Accuracy	Same as sample clock
Vertical resolution IQ	16 bit
SNR improvement relative to direct mode	3 dB per octave of decimation (nom.) (e.g. 12 dB @ DDC by 16)
Decimation filter passband ripple	< 0.0025 dB (nom) for decimation factor 4 < 0.005 dB (nom) for decimation factors 8,16 < 0.0065 dB (nom) for decimation factors 32, 64, 128, 256, 512

The following combinations of sample rate, DDC and decimation factor are supported:

ADC Sample rate	DDC	Decimation factor	Sample rate after decimation	Data format	Data rate	Modulation bandwidth
32 GSa/s [1]	Off	1	32 GSa/s	10-bit, real	320 Gbit/s	12.5 GHz
32 GSa/s [1]	Off	2	16 GSa/s	16-bit, real	256 Gbit/s	6.4 GHz [2]
32 GSa/s [1]	Off	4	8 GSa/s	16-bit, real	128 Gbit/s	3.2 GHz [2]
32 GSa/s [1]	On	4, 8, …, 512	8, 4, …, 0.0625 GSa/s	16 bit I + 16 bit Q	256, 128, …, 2 Gbit/s	6.4, 3.2, …, 0.05 GHz
16 GSa/s	Off	1	16 GSa/s	10-bit, real	160 Gbit/s	6.4 GHz
16 GSa/s	Off	2	8 GSa/s	16-bit, real	128 Gbit/s	3.2 GHz [2]
16 GSa/s	Off	4	4 GSa/s	16-bit, real	64 Gbit/s	1.6 GHz [2]

16 GSa/s	On	4, 8, …, 512	4, 2, …, 0.03125 GSa/s	16 bit I + 16 bit Q	128, 64, …, 1 Gbit/s	3.2, 1.6, …, 0.025 GHz

[1] In 32 GSa/s mode, 2 ODI links per ADC channel are required.
[2] Might require external Low-Pass Filter (LPF) to limit the bandwidth to 1st Nyquist band or might require external High-pass filter (HPF) to limit the bandwidth to 2nd Nyquist band.

Instrument modes

The M8131A supports the following operating modes:

Continuous Capture / Streaming (available in direct and DDC mode)	
Capture to built-in memory	For each trigger event, the configured number of samples is captured. Subsequent triggers overwrite memory. Capture to built-in memory is also possible while streaming is in progress (e.g. to check if the input signal is still available)
Streaming over ODI	The first trigger event starts acquisition of samples, which are streamed over ODI until stopped by the user
Segmented Streaming (only available in DDC mode; requires Options SEG & DDC)	
Capture to built-in memory	For a trigger event, the configured number of samples is captured. The first sample of the segment is timestamped.
Streaming over ODI	For each trigger event, the configured number of samples is streamed over ODI. Each segment is preceeded with a timestamp. The first sample of each segment is timestamped. The user can choose between “fixed” and “variable” segment size. With “variable” segment size, it is guaranteed that all signals that satisfy the trigger/gate condition are streamed (i.e. 100% probability of intercept)

Capture memory

Built-in capture memory	400 MSa/ch. 16 GSa/s, DDC Off, no decimation (10-bit samples) 250 MSa/ch. 16 GSa/s, DDC Off, with decimation (16-bit samples) 125 MSa/ch. 16 GSa/s, DDC On & decimation (16-bit I & 16-bit Q sample pairs) 800 MSa/ch. 32 GSa/s, DDC Off, no decimation (10-bit samples) 500 MSa/ch. 32 GSa/s, DDC Off, with decimation (16-bit samples) 250 MSa/ch. 32 GSa/s, DDC On & decimation (16-bit I & 16-bit Q sample pairs)

Upload speed

The upload speed is measured by transferring the captured waveform samples from the M8131A to the controlling PC's memory.

Upload speed. USB using SCPI	~5.5 MBytes/s (meas.)
Upload speed. PCIe using SCPI	~45 MBytes/s (meas.)

System Requirements

Operating System	Windows 8.1, 10 (64-bit)
Connection to AXIe hardware	PCIe or USB or Thunderbolt

General Characteristics [1]

Power consumption	350 W (nom.)
Operating temperature	0 °C to +40 °C
Operating humidity	5% to 80% relative humidity, non-condensing
Operating altitude	Up to 3000 m
Storage temperature	-40 °C to +70 °C
Storage humidity	5% to 80% relative humidity, non-condensing
Operating random vibration [2]	Type tested at 5 to 500 Hz, 0.21 g RMS
Survival random vibration [2]	Type tested at 5 to 500 Hz, 2.09 g RMS
Stored states	User Configuration and factory default
Power on state	Default
Interface to controlling PC	PCIe or USB or Thunderbolt (see AXIe specification)
Form factor	2-slot AXIe module
Dimensions (H x W x D)	60 mm x 322.5 mm x 281.5 mm
Weight	5 kg
Safety tested acc. to	IEC61010-1, ANSI/UL61010, CSA22.2 No. 61010-1 certified
EMC tested acc. to	IEC61326
Warm-up time	15 min
Calibration interval	1 year recommended
Cooling requirements	Choose a location that provides at least 80 mm of clearance at rear, and at least 30 mm of clearance at each side.

[1] Samples of this product have been tested in accordance with the Keysight Environmental Test Manual and verified to be robust against environmental stresses of storage, transportation, and end-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude, and power line conditions.
[2] Test methods are according to IEC 60068-2-64 and levels are similar to MIL-PRF-28800F Class 3.

Definitions

Specification (spec.)

The warranted performance of a calibrated instrument that has been stored for a minimum of 2 hours within the operating temperature range of 0 °C to 40 °C and a 15-minute warm up period. Within +/- 10°C after auto calibration. All specifications include measurement uncertainty and were created in compliance with ISO-17025 methods. Data published in this document are specifications (spec) only where specifically indicated.

Typical (typ.)

The characteristic performance, which 80% or more of manufactured instruments will meet. This data is not warranted, does not include measurement uncertainty, and is valid only at room temperature (approximately 23 °C).

Nominal (nom.)

The mean or average characteristic performance, or the value of an attribute that is determined by design such as a connector type, physical dimension, or operating speed. This data is not warranted and is measured at room temperature (approximately 23 °C).

Measured (meas.)

An attribute measured during development for purposes of communicating the expected performance. This data is not warranted and is measured at room temperature (approximately 23 °C).

Accuracy

Represents the traceable accuracy of a specified parameter. Includes measurement error and timebase error, and calibration source uncertainty.

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