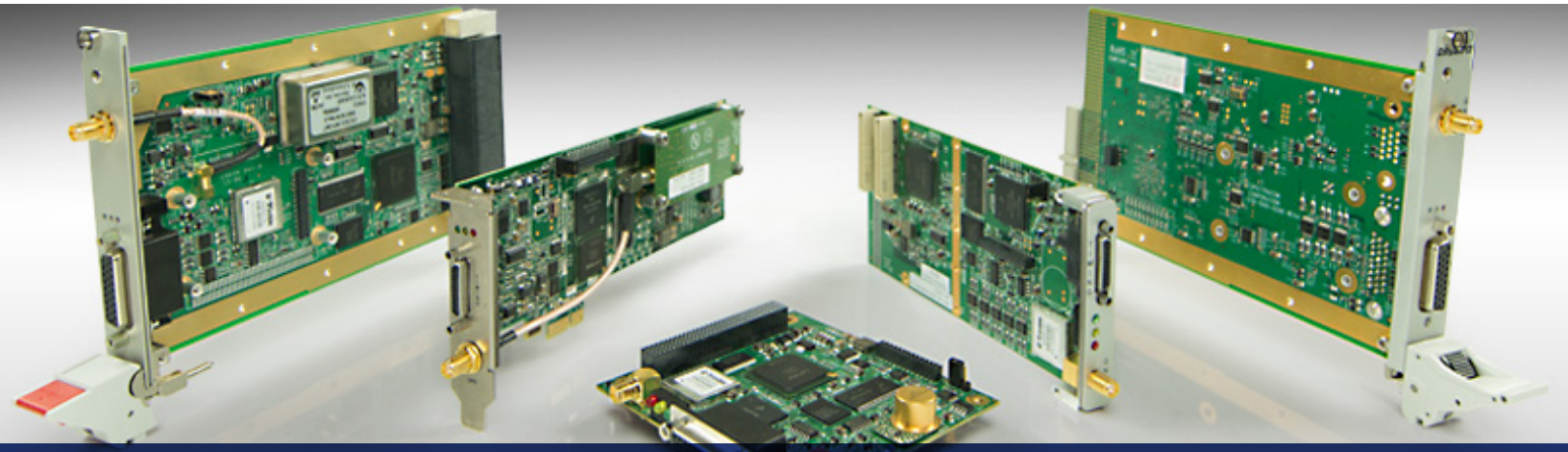
The Global Leader in Resilient **PNT**

# TSync Time Code Processors



## Form Factors

- PCIe, cPCI, PCI-104, PMC, VPX
- Others available upon request
- Rugged design
- Conduction-cooled ready
- Conformal coating available

## Available References

- GNSS synchronization (multi-constellation)
- SAASM GPS option
- IRIG timecode
- 1PPS
- Internal clock

## Timing Functions

- IRIG timecode generator
- 1PPS and programmable periodic output
- 10 MHz output
- Event time-tagging
- Time-match/alarm signal

Orolia TSync time code processors are complete synchronization systems on circuit cards ready for easy integration into mission-critical applications.

Each board has an onboard clock/oscillator that can phase-lock to a wide variety of external timing references and provides 5 ns resolution to the timekeeping hardware. The user can prioritize multiple references so if one is lost the unit will automatically switch to the next. The oscillator can be its own reference when it “freewheels” in the absence of a valid external synchronization source. For applications where accuracy in this “holdover” conditional is essential, an upgrade to a higher precision ovenized crystal oscillator (OCXO) is available.

Some models are conduction-cooled ready with a thermal frame option

Four user-programmable time tag inputs may be used for multiple event capture at 10,000 events per second. Additionally, four programmable time match outputs are provided. Key to the TSync functionality is the ability to generate interrupts. Using a Orolia driver package available for the latest versions of popular operating systems, you may configure your board using interrupt-driven algorithms to support your unique applications.

Orolia TSync boards offer a high degree of ruggedness, customization and field upgradability. If a new application or change in deployment requires a different feature set, we can usually accommodate it.

## Internal Timekeeping

### Disciplined On-Board Clock

- Frequency: 200 MHz
- Resolution: 5 ns
- Sync Sources: GNSS, IRIG, 1 PPS inputs

## Reference Inputs

### GNSS Reference

- Frequency: GPS L1 (1575.42 MHz), GLONASS L1 (1602 MHz); contact the factory for compatibility with QZSS (1572.42 MHz), BeiDou (1561.1 MHz) and Galileo (1575.42 MHz)

### Internal GNSS Receiver Option

- Front panel connector: SMA jack (+5 V at 30 mA max supplied to power antenna pre-amp)
- Antenna sold separately
- SMA to Type N adapter cable included

### External GNSS Receiver/ Antenna Option (PCIe and cPCI Only)

- Size: 45 mm dia., 72.55 mm H (3.74" dia., 2.85" H)
- Pole mount included
- Operating temperature: -40°C to 85°C (-40°F to +185°F)
- Cable: 30.5 M (100') included, 92 M (300') max., 9 mm (0.35"dia.); Connectors: 20 mm (0.79") at antenna end, DB15 at board end, with adapter cable

### SAASM GPS Receiver Option (cPCI and VPX Only)

- Antenna sold separately
- SMA to Type N adapter cable included with convection cooled models
- See table for specs

### IRIG

#### Code Format (AM or DCLS)

IRIG A, IRIG B, IRIG G, NASA36 (auto-detect), IEEE 1344/C37.118 (selectable)

#### AM

- Amplitude: 500 mV p-p min,10 V p-p max
- Modulation Ratio: 2:1 min, 6:1 max
- Input Impedance: >10 K Ohms
- Common mode voltage: ±150 V DC max
- Input stability: Better than 100 ppm

#### DCLS (Differential or Single Ended)

- Differential amplitude: 200 mV p-p min, 5 V p-p max - 7V to +12 V DC max common mode voltage (RS-485 compatible)
- Single ended amplitude: +1.3V VIL min, +2 V VIH max (TTL compatible)

### 1PPS Input

- Amplitude: 0 V to +5.5 V, +0.8 V VIL, +2.0 V VIH
- 1 Hz Pulse, rising edge or falling edge active (selectable)
- 100 ns minimum pulse width
- Input Impedence: <150 pF capacitive

### General Inputs (x4)

Event Time-Tag Input

- Amplitude: 0 V to +5.5 V, +0.8 V VIL, +2.0 V VIH
- Polarity (selectable): Positive or negative
- Pulse width: 50 ns min
- Repetition rate: More than 10,000 events per second
- Resolution: 5 ns

## Outputs

### IRIG

#### Code Format (AM or DCLS)

IRIG A, IRIG B, IRIG E, IRIG G, NASA36, IEEE 1344

#### AM

- Amplitude (adjustable): 500 mV p-p min, 6 V p-p max into 50 ohms
- Modulation ratio: 3:1
- Output impedance: 50 Ohms

#### DCLS

- Differential amplitude: 1.5 V p-p min, 3.3V p-p max, ±1.5 V min,1.8 V max common mode voltage (RS-485 compatible)
- Single ended amplitude: (100 Ohm Load) +0.5V VOL max, +2.5 V VOH min (TTL compatible)

### 1PPS

- Signal level: TTL compatible, 4.3 V minimum, base-to-peak into 50 (for PCIe only: TTL compatible, 2.2 V minimum, base-to-peak into high impedance)
- Pulse width: Configurable Pulse width (200 ms by default)
- Rise time:< 10 ns
- Accuracy: See table

### General Outputs (x4)

#### Periodic Output

- Amplitude: TTL compatible, 4.3 V minimum, base-to-peak into 50 (for PCIe only: TTL compatible, 2.2 V minimum, base-to-peak into high impedance)
- Period: 100 ns min, 60 s max in 20 ns steps (10 MHz – 0.17 Hz)
- Pulse width: 20 ns min, 999 ms max in 20 ns steps
- Polarity (selectable): Positive or negative

### Internal SAASM GPS Reference (cPCI and VPX Only):

| | Value |
|---|---|
| SAASM GPS Receiver | MPE-S Type II GB-GRAM |
| Frequency | L1 (1575.42 MHz) and L2 (1227.6 MHz) simultaneous<br>L1- C/A, P(Y)<br>L2 - P(Y) |
| Satellite Tracking | 1 to 12 |
| TTFF - Time to First Fix (Synchronization Time) | Cold Start (with almanac download): 15 minutes<br>Cold Start (no almanac download): 5 minutes<br>Warm Start: 90 seconds<br>Hot Start: 10 seconds |
| TTSF - Time to Subsequent Fix (Reacquisition Time) | < 20 seconds, Off or Stby < 15 minutes<br>< 25 seconds, Off or Stby < 60 minutes<br>< 70 seconds, Off < 60 minutes |
| Antenna Connector | Convection Cooled: SMA Jack (+3.3 V @ 9 mA to 60 mA)<br>Conduction Cooled: MMCX Jack (+3.3 V @ 9 mA to 60 mA) |
| 1 PPS Accuracy | ±100 ns |
| Key Fill | DS102 standard, DS101 optional |
| Backup Battery | SAASM I/O connector or P1-VBAT, VPX P1 connector |

### 1 PPS Output:

| | TCXO | OCXO | OCXO Rugged Option (cPCI & VPX only) |
|---|---|---|---|
| Accuracy to UTC (1-sigma locked to GPS) | ±50 ns | ±50 ns | ±25 ns |
| Holdover (constant temp after 2 weeks of GPS lock) | | | |
| After 4 hours | 12 µs | 3 µs | 1 µs |
| After 24 hours | 450 µs | 100 µs | 25 µs |

### 10 MHz Frequency Output:

| | TCXO | OCXO | OCXO Rugged Option (cPCI & VPX only) |
|---|---|---|---|
| Accuracy (average over 24 hours when GPS locked) | $1x10^{-11}$ | $5x10^{-12}$ | $2x10^{-12}$ |
| Medium Term Stability (without GPS after 2 weeks of GPS lock) | $1x10^{-8}$/ day | $2x10^{-9}$/ day | $5x10^{-10}$/day |
| Phase Noise (dBc/Hz) | | | |
| @1 Hz | — | -90 | — |
| @10 Hz | — | -113 | -120 |
| @100 Hz | -110 | -120 | -135 |
| @1 KHz | -135 | -140 | -135 |
| @10 KHz | -140 | -150 | -145 |
| Signal Waveform & Levels: +13 dBm ±3 dB into 50 ohm, BNC | | | |

### Time-Match/Alarm Output
- Amplitude: TTL compatible, 4.3 minimum, base-to-peak into 50
- 2.2 V minimum, base-to-peak into high impedance)
- Range: 100 days in 5 ns steps

### 10 MHz Output (Sine Wave)
- Harmonics: < -40 dBc
- Spurious: < -70 dBc
- Other specifications: See table

### 10 MHz LVDS Clocks via P2 Connector (VPX only)
- Four (4) LVDS differential pairs
- Impedance: 100 ohm
- Duty cycle: 50%
- Rise time: < 10 ns

## General

### PCIe Specifications
- Full-height mounting bracket provided
- Bus interface: Low-profile PCIe x1, Rev 1.1

### PMC Specifications
- Single size CMC (common mezzanine card) 149 mm x 74 mm
- Bus interface: Universal signaling voltage 3.3 V/5 V
- Bus speed: 32bit address @ 33/66 MHz

### cPCI Specifications
- 3U Compact PCI (cPCI) compliant to PICMG 2.0 r3.0 100 mm x 160 mm (3U card size)
- Bus interface: Universal signaling voltage 3.3 V/5 V
- Bus speed: 32bit address @ 33/66 MHz

### VPX Specifications
- 3U VPX form-factor compliant to VITA-46
- 3.9" x 6.3" (100 mm x 160 mm)
- Connectors to VITA 46.0 for P0, P1, and P2
- Bus interface: PCIe x1, Rev 1.1

### PCI-104 Specifications
- Compliant to PCI-104 spec, rev 1.1
- Compliant to PCI spec, rev 2.2
- DIP switch selectable PCI-104 stack level
- Bus interface: Universal signaling voltage 3.3 V/5 V
- Bus speed: 32bit address @ 33/66 MHz

### Conduction Cooling (cPCI and VPX only)
- Per ANSI/VITA 30.1-2002 (cPCI)
- Per VITA 46/IEEE 1101.2 (VPX)
- Thermal frame available by request
- Component elevations available for custom thermal frame design

### Power
See table below.

### Environmental

#### Temperature
- Operating: -40°C to 80°C (-40°F to +176°F) at card edge with conduction cooled frame
- Storage: -40°C to 85°C (-40°F to +185°F)

#### Humidity
- Operating & storage: 95% RH at 60°C for 5 cycles of 48 hours/ cycle

### Physical

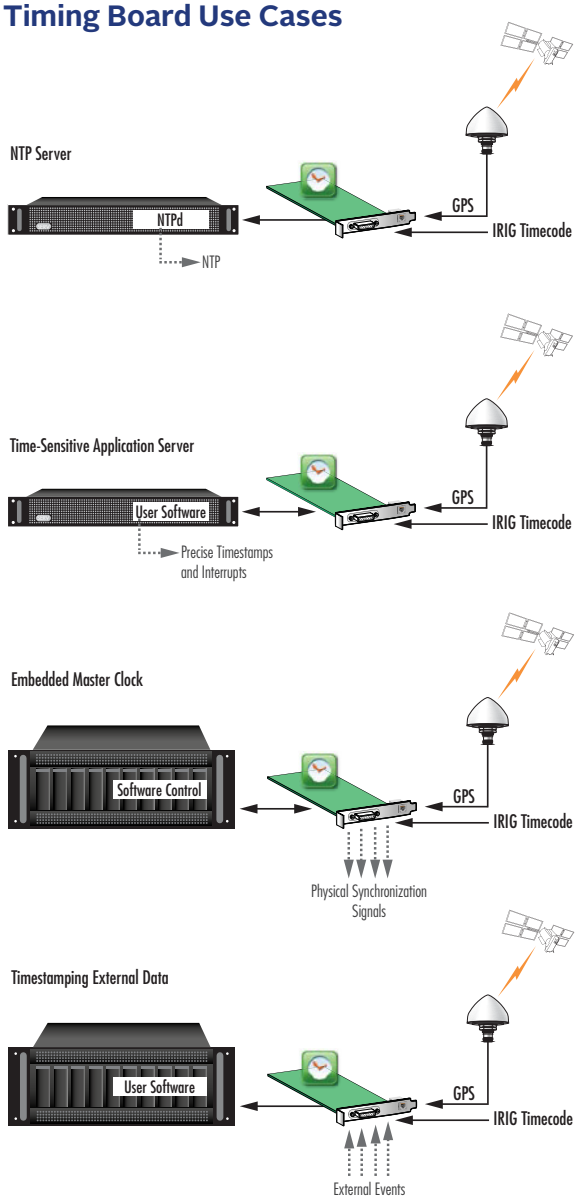
#### Weight (base configurations)
- PCIe: 4.3 oz/122 g
- PMC: 3.1 oz/88 g
- cPCI: 6.1 oz/173 g (without thermo frame), 11.4 oz/323 g (with thermo frame)
- VPX: 6.3 oz/179 g (without thermo frame), 11.6 oz/329 g (with thermo frame)
- PCI-104: 3.4 oz/96 g

### Safety & EMI
Certifications: RoHS, CE, FCC Class A

### Drivers
Linux* 64/32 bit, Windows 7 64/32 bit, Windows Embedded

*Contact sales for specific kernel versions

## Timing Board Use Cases




## Power:

| | +5 VDC | +3.3 VDC | +12 VDC | -12 VDC |
|---|---|---|---|---|
| PCIe | — | ±5% @ 0.7A typ | ±8% @ 0.2A typ | — |
| PMC | ±5% @ 1.4A typ | ±5% @ 0.7A typ | ±8% @ 0.2A typ | ±5% @ 0.2A typ |
| cPCI | ±5% @ 1.4A typ | ±5% @ 0.7A typ | ±8% @ 0.2A typ | ±5% @ 0.2A typ |
| PCI-104 | ±5% @ 1.4A typ | ±5% @ 0.7A typ | ±8% @ 0.2A typ | ±5% @ 0.2A typ |
| VPX | Vs3: +5%/-2.5% @ 0.4A typical TCXO, OCXO options @ 0.6A typical rugged OCXO option @ 1.4A maximum rugged OCXO option warm-up | Vs2: +5%/-2% @ 0.85A typ | Vs1: ±5% @ 0.2A typ | 12V_AUX: -±5% @ 0.2A typ |

**TSync-PCIe**

**TSync-PMC**

**TSync-cPCI**

**TSync-VPX**

**TSync-PCI-104**

## Ordering Information*

Orolia's TSync timing boards come in several configurations depending on the bus type/form factor. Variations include the precision of internal timekeeping, synchronization to external references and interconnections to external devices.

### Model Number

TSync-AAAA-X-Y-Z
AAAA = Form Factor
X= Custom Options
Y=Internal Oscillator
Z=External Reference

### Options

**Premium Breakout Cable Upgrade:**
Replaces basic breakout cable for all available inputs and outputs.

*For more information about external connections (adapters, breakout cables, antennas, etc.) please see the TSync Configurations & Ordering Information datasheet.

| Form Factor/Bus Type (AAAA) | Custom Options (X) | | | Internal Options (Y) | | | External Reference (Z) | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 0=NONE | 1=TF | 3=CC | 0=TCXO | 1=OCXO | 2=Rugged OCXO | 0=IRIG or Other | 1=Internal GPS/ GNSS | 2=External GPS/GNSS | 3=SAASM GPS |
| PCIe (PCI Express) | x | | x | x | x | | x | x | x | |
| PMC (PCI mezzanine card) | x | x | x | x | x | | x | x | | |
| cPCI (compact PCI) | x | x | x | x | x | x | x | x | x | x |
| VPX | x | | x | x | x | x | x | x | | x |
| PCI-104 | x | | x | x | x | | x | x | | |

TF = Thermal Frame
CC = Conformal Coating



21 September, 2018 - TSync (C)
Specifications subject to change or improvement without notice