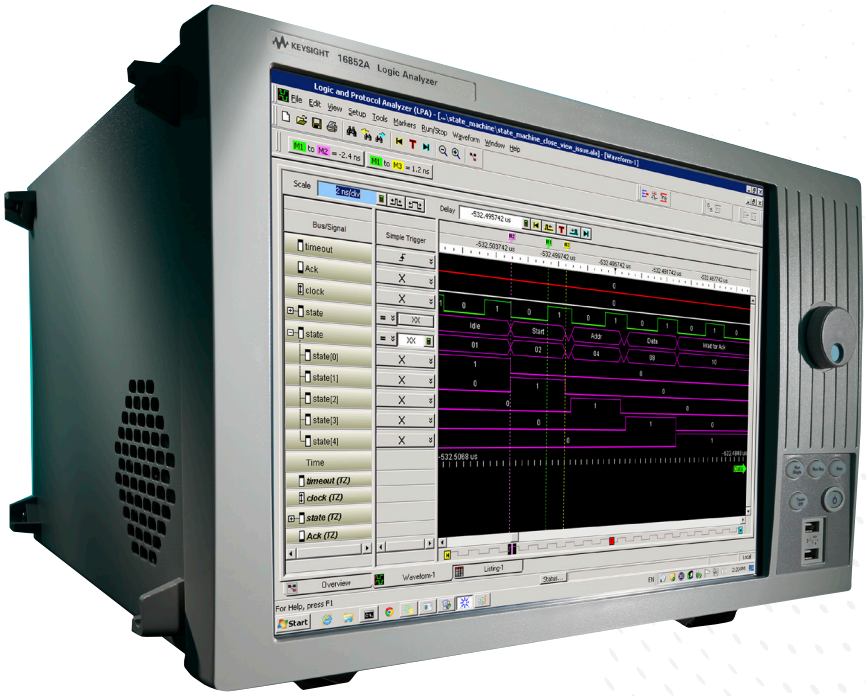
DATA SHEET

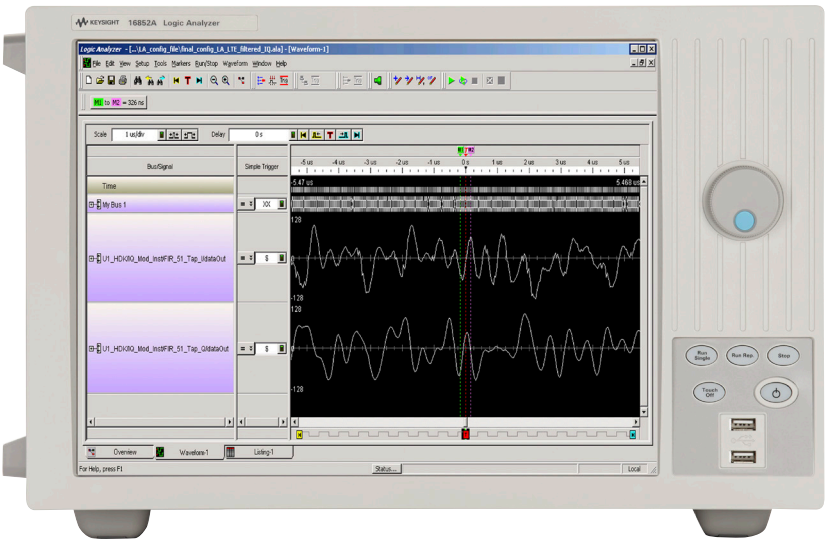
16850 Series
Portable Logic Analyzers



KEYSIGHT TECHNOLOGIES

16850 Series Portable Logic Analyzer Selection Guide

- 2.5 GHz timing capture with up to 128 M sample memory for finding elusive problems quickly, even far from the trigger point
- Up to 1.4 GHz trigger sequencer speed for state and timing capture
- Single-ended and differential probing for the widest range of supported technologies
- 80 ps resolution (12.5 GHz) Timing Zoom with 256 K samples allows you to observe signal timing in proximity to the trigger point
- Up to 1.4 Gbps state data rate tracks high speed parallel and serial buses in your design
- Gain signal integrity insight on all channels using exclusive “eye scan”
- Four models with 34/68/102/136 channels provide the measurement flexibility for a wide range of applications
- Application support for many aspects of today’s complex designs bring target insight FPGA dynamic probe, and digital VSA (vector signal analysis)
- Powerful, customizable triggering quickly isolates problems
- Proven, easy to use interface speeds debug
- Standard 15 inch touch screen allows viewing of multiple buses and signals



Specifications and characteristics	16851A	16852A	16853A	16854A
Channels	34	68	102	136
Maximum timing sample rate (half/full channel)	5 GHz (200 ps) with up to 256 M depth			
	2.5 GHz (400 ps) with up to 128 M depth			
High-speed timing zoom	12.5 GHz (80 ps) with 256 Kb depth			
Trigger sequencer	1.4 GHz			
Maximum state clock rate	700 MHz with Option 700			
	350 MHz standard			
Maximum state data rate	1400 Mb/s with Option 700			
	700 Mb/s standard			
Maximum memory depth	2 M default			
	4 M with Option 004			
	8 M with Option 008			
	16 M with Option 016			
	32 M with Option 032			
	64 M with Option 064			
	128 M with Option 128			
Supported signal types	Single-ended, differential			
Automated threshold/sample position	Yes			
Simultaneous eye diagrams, all channels	Yes			
Probe compatibility	Direct connect single-ended flying lead			
	Direct connect Mictor probe			
	90-pin connector single-ended and differential probes for flying lead, Mictor, Soft Touch, Soft Touch Pro, and Samtec connections (used in conjunction with a U4201A cable)			
	Select DDR2/3 BGA probes and probe cables			
	Select DDR3 Addr/Cmd slot interposer probes			

Industry's Fastest Timing Capture with Deep Memory – for Fast Digital System Debug

The Keysight Technologies, Inc. 16850 Series portable logic analyzers offer the highest performance, with deep, high speed timing and state measurements, combined with the applications and usability your digital development teams need to debug their modern systems – and at a great price.

The logic analyzer's timing and state acquisition gives you the power to:

- Observe timing relationships far away from the trigger point using 2.5 GHz (400 ps)/5 GHz (200 ps) full/half channel timing with up to 128 M samples
- Measure more precise timing relationships in the vicinity of the trigger point using 12.5 GHz (80 ps) Timing Zoom (256 K samples)
- Find anomalies separated in time with memory depths upgradable to 128 M
- Probe a variety of technologies with single-ended and differential attachment options with the highest signal integrity
- Buy what you need today and upgrade in the future. 16850 Series logic analyzers come with independent upgrades for state speed and memory depth
- Sample synchronous buses up to 1400 Mbps data rates accurately using eye scan to automatically adjust threshold and setup/hold
- Easily track problems from symptom to root cause across several measurement modes by viewing time-correlated data in waveform/chart, listing, inverse assembly, source code, or compare display
- Identify potential signal integrity issues on high data rate signals by observing an analog view of all input channels via logic analyzer probing with "eye scan"
- Set up triggers quickly and confidently with intuitive, "simple," "quick," and "advanced" triggering options
- Time correlate and import oscilloscope/mixed-signal traces into the logic analyzer Waveform window for even greater system insight

Figure 1. With four models to choose from, and options to upgrade state speed and memory depth, you can get a logic analyzer with measurement capabilities that meet your needs.

Automate the capture of internal FPGA signals

16850 Series logic analyzers, used with the FPGA Dynamic Probe, let you probe internal FPGA nets on Xilinx and Altera devices with deep memory and through an automated process

- No block RAM required
- Move probe points without stopping the FPGA or changing design timing
- Import signal names automatically from the FPGA design
- Automatically map FPGA pins to logic analyzer input channels (Xilinx)
- B4655A (Xilinx) B4656A (Altera)

Decode DDR2/3 memory Addr/Cmd buses and perform compliance and performance analysis

Eye Scan to Set Sample Points and to View Signal Integrity

Automate measurement setup and quickly gain diagnostic clues

16850 Series logic analyzers make it easy for you to get up and running quickly by automating your measurement setup process. In addition, the logic analyzer's setup/hold window (or sampling position) and threshold voltage settings are automatically determined so you can capture data on high-speed buses with the highest accuracy. Auto Threshold and Sample Position mode allow you to...

- Obtain accurate and reliable measurements
- Save time during measurement setup
- Gain diagnostic clues and identify problem signals quickly
- Scan all signals and buses simultaneously or just a few
- View results as a composite display or as individual signals
- See skew between signals and buses
- Find and fix inappropriate clock thresholds
- Measure data valid windows
- Identify signal integrity problems related to rise times, fall times, data valid window widths

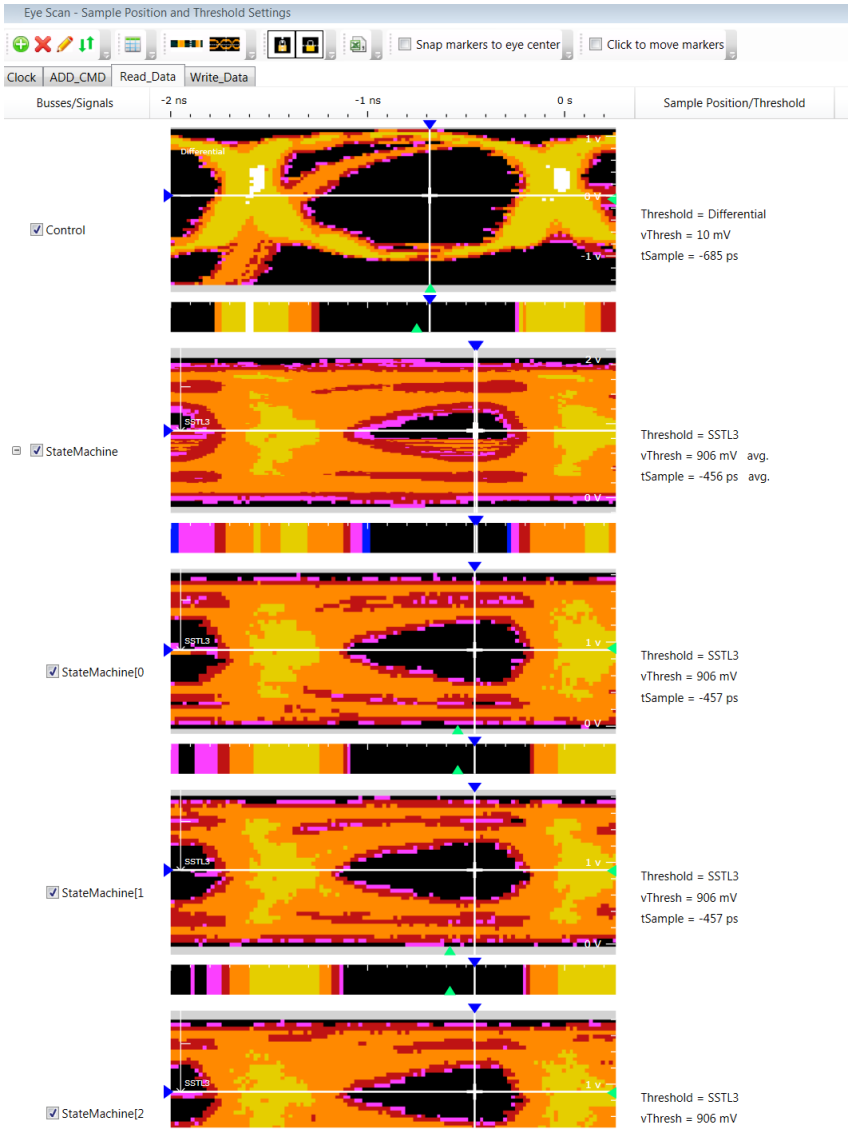


Figure 2. Eye scan automatically sets sample positions for accurate state capture and also provides a signal integrity view of each input signal, without the need for an oscilloscope.

Identify problem signals over one hundred channels simultaneously

As timing and voltage margins continue to shrink, confidence in signal integrity becomes an increasingly vital requirement in the design validation process. Eye scan lets you acquire signal integrity information on all the buses in your design, under a wide variety of operating conditions, in a matter of minutes. Identify problem signals quickly for further investigation with an oscilloscope. Results can be viewed for each individual signal or as a composite of multiple signals or buses.

16850 Series Logic Analyzer Specifications and Characteristics

	16851A	16852A	16853A	16854A
Number of channels	34 (1 clock + 1 clock qualifier)	68 (1 clock + 3 clock qualifiers)	102 (1 clock + 3 clock qualifiers)	136 (1 clock + 3 clock qualifiers)

Deep timing (asynchronous) sampling mode	Conventional and transitional timing (up to 128 M depth)
Maximum sample rate in full channel mode (nom)	2.5 GHz
Maximum sample rate in half channel mode (nom)	5 GHz
Sample period on all channels (nom)	400 ps to 10 ns
Sample period in half channel mode (nom)	200 ps
Minimum data pulse width (nom)	1 sample period + 200 ps
Maximum time between transitions (nom)	66 days
Time interval accuracy within a 16 channel pod (typ) [1]	± (1 sample period + 130 ps + 0.01% of time interval reading)
Time interval accuracy across 16 channel pods (typ) [1]	± (1 sample period + 400 ps + 0.01% of time interval reading)

1. With single-ended flying lead and Soft Touch Pro probes.

Timing zoom (captured simultaneously with timing or state sampling mode capture)	
Timing analysis sample rate (nom)	12.5 GHz (80 ps sample resolution)
Time interval accuracy (nom)	
– Within a 16 channel block	– ± (80 ps + 130 ps + 0.01% of time interval reading)
– Between 16 channel blocks	– ± (80 ps + 400 ps + 0.01% of time interval reading)
Memory depth (nom)	256 K samples
Trigger position (nom)	Start, center, end, or user-defined
Minimum data pulse width (nom)	1 sample period + 200 ps

State (synchronous) sampling mode	
Maximum state data rate – base (spec)	700 Mb/s using both edges of clock (spec)
Maximum state data rate – Option 700 (spec)	1.4 Gb/s using both edges of clock (spec)
Maximum state clock frequency – single edge clocking – base (typ)	350 MHz
Maximum state clock frequency – single edge clocking – Option 700 (typ)	700 MHz
Minimum state clock frequency (typ) [1]	12.5 MHz (single edge)
	6.25 MHz (both edges)
Minimum data valid window (typ) [2]	160 ps
Sample position adjustment resolution (typ)	20 ps
Sample position adjustment accuracy (typ)	± 150 ps
Minimum data valid window (typ) [1]	160 ps
Minimum setup time (typ)	80 ps
Minimum hold time (typ)	80 ps
Minimum eye height (typ)	160 mV
Sample position adjustment range (typ)	7 ns
Minimum state clock pulse width single edge (typ)	200 ps
Minimum time between active clock edges – standard (typ)	1429 ps
Minimum time between active clock edges – Option 700 (typ)	714 ps
Maximum time between active clock edges (typ) [1]	80 ns (single edge)
Clock qualifier setup time (typ)	200 ps
Clock qualifier hold time (typ)	200 ps
Time tag resolution (typ)	80 ps
Maximum time count between stored states (nom)	66 days

1. Clock can pause for up to 66 days once every 8 or more edges.
2. Dependent on probing system.

16850 Series Logic Analyzer Specifications and Characteristics (Continued)

Trigger characteristics (conventional timing, transitional timing, and state sampling modes)	
Maximum trigger sequence speed (standard) (nom)	700 MHz (state), 1.4 GHz (timing)
Maximum trigger sequence speed (option 700) (nom)	1.4 GHz
Maximum trigger sequence levels (nom)	8
Trigger sequence level branching (nom)	Arbitrary 4-way if/then/else
Trigger position (nom)	Start, center, end or user-defined
Trigger resources (nom)	16 patterns evaluated as =, !=, >, >=, <, <=
	8 double-bounded ranges evaluated as in range, not in range
	4 edge detectors in timing, 3 in transitional timing
	1 occurrence counter per sequence level
	1 timer
	3 flags
	1 arm in
Trigger resource Boolean conditions (nom)	Arbitrary Boolean combinations
Trigger actions (nom)	Go To
	Trigger and fill memory
	Trigger and Go To
	Trigger, send e-mail, and fill memory
	Occurrence counter reset
Store qualification actions (nom)	Default (global) and per sequence level
	Store/don't store sample
	Turn on/off default storing
Timer actions	Start from reset
	Stop and reset
	Pause
	Resume
Flag actions	Set
	Clear
	Pulse set
	Pulse clear
Maximum occurrence counter (nom)	999,999,999
Maximum pattern width (nom)	128 bits – single label
Maximum range width (nom)	64 bits
Timers range (nom)	200 * sample clock period to 27 hours
Timer resolution (nom)	5 ns
Timer accuracy (typ)	± (8 * sample clock period + 2 ns + 0.01%)
Timer reset latency (nom)	80 * sample clock period
General	
Input signal amplitude V_{amptd} (typ)	≥ 350 mV
Supported signal types	Single-ended and differential
Voltage threshold (typ)	–5 V to +5 V
Threshold resolution (typ)	2 mV
Threshold accuracy (typ)	± (30 mV + 1% of setting)
Threshold setting granularity	Individual threshold for each channel

1. Specification (spec): Represents warranted performance of a calibrated instrument that has been stored for a minimum of 2 hours within the operating temperature range of 0 to 40 °C, unless otherwise stated, and after a 45-minute warm-up period. The specifications include measurement uncertainty.
2. Typical (typ): Represents characteristic performance, which 80% of the instruments manufactured will meet. This data is not warranted, does not include measurement uncertainty, and is valid only at room temperature (approximately 25 °C).
3. Nominal (nom): The expected mean or average performance, or an attribute whose performance is by design, such as the 50 Ω connector. This data is not warranted and is measured at room temperature (approximately 25 °C).
4. Measured (meas): An attribute measured during the design phase for purposes of communicating expected performance, such as amplitude drift versus time. This data is not warranted and is measured at room temperature (approximately 25 °C).

Unleash the Complementary Power of a Logic Analyzer and an Oscilloscope

Seamless oscilloscope integration with View Scope

Easily make time-correlated measurements between Keysight logic analyzers and oscilloscopes. The time-correlated logic analyzer and oscilloscope waveforms are integrated into a single logic analyzer waveform display for easy viewing and analysis. You can also trigger the oscilloscope from the logic analyzer (or vice versa), automatically de-skew the waveforms and maintain marker tracking between the two instruments. View Scope allows you to perform the following more effectively:

- Validate signal integrity
- Track down problems caused by signal integrity
- Validate correct operation of A/D and D/A converters
- Validate correct logical and timing relationships between the analog and digital portions of a design

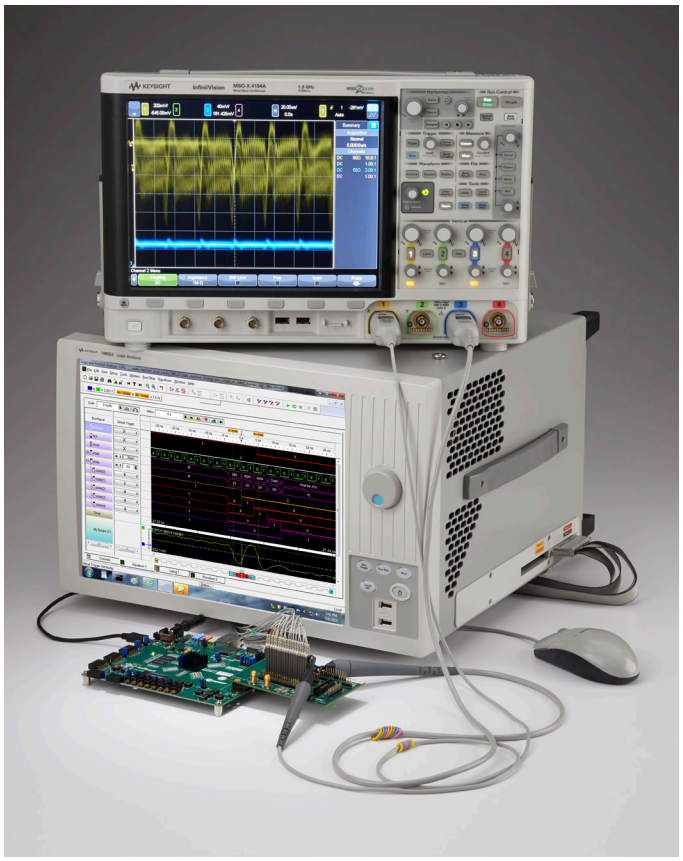


Figure 3. View Scope seamlessly integrates your scope and logic analyzer waveforms into a single display.

Connection

The Keysight logic analyzer and oscilloscope can be physically connected with standard BNC and LAN connections. Two BNC cables are connected for cross triggering, and the LAN connection is used to transfer data between the instruments. The View Scope correlation software is standard in the logic analyzer's application software version 3.50 or higher. The View Scope software includes:

- Ability to import some or all of the captured oscilloscope waveforms
- Auto scaling of the scope waveforms for the best fit in the logic analyzer display

Feature	Benefit
Automated setup	Quickly get to your first measurement using the logic analyzer's Help wizard for easy setup, regardless of which supported Keysight oscilloscope you connect to.
Integrated waveform display	Instantly validate the logical and timing relationships between the analog and digital portions of your design. View oscilloscope and logic analyzer waveforms integrated into a single logic analyzer waveform display.
Automatic measurement de-skew	Save time and gain confidence in measurement results with measurements that are automatically de-skewed in time.
Cross trigger the logic analyzer and oscilloscope	Start your debug approach from either the analog or digital domain with the flexibility to trigger the oscilloscope from the logic analyzer (or vice versa).
Tracking markers	Precisely relate information on the oscilloscope's display to the corresponding point in time on the logic analyzer display with tracking markers. The oscilloscope's time markers automatically track adjustments of the logic analyzer's global markers.

Get Instant Insight into your Design with Multiple Views and Analysis Tools

Acquisition and analysis tools provide rapid insight into your toughest debug problems

When you want to understand what your target is doing and why, you need acquisition and analysis tools that rapidly consolidate data and provide insight into your system's behavior.

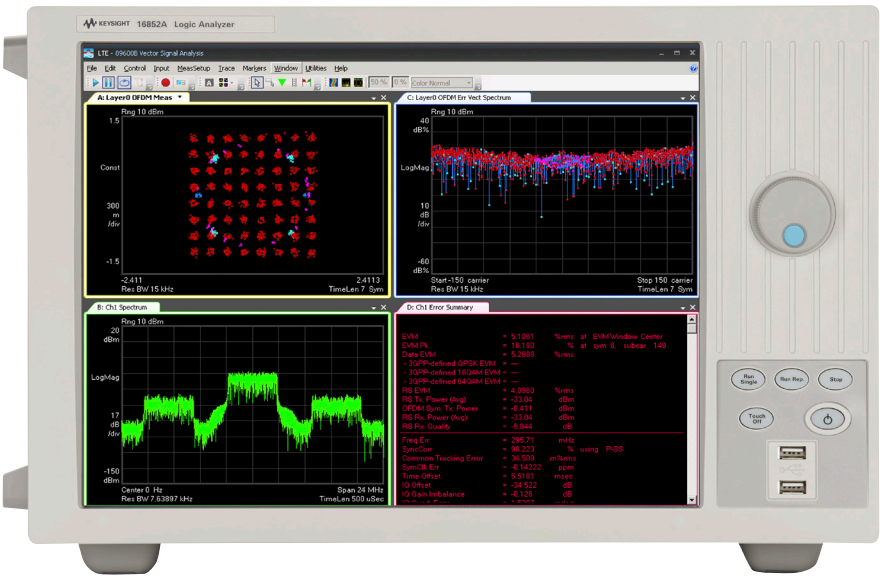


Figure 4. Perform in-depth time, frequency and modulation domain analysis on your digital baseband and IF signals with Keysight's 89600 Vector Signal Analysis software, running on the logic analyzer.

Optional analysis and automated measurement packages	
B4655A FPGA Dynamic Probe (Xilinx), B4656A FPGA Dynamic Probe (Altera)	Gain unprecedented visibility into your FPGA's internal activity. Make incremental real-time measurements in seconds without stopping the FPGA, changing the design or modifying design timing. Quickly set up the logic analyzer with automatic pin mapping and signal bus naming by leveraging work you did in your design environment. www.keysight.com/find/fpga
89601B-300 digital vector signal analysis, hardware connectivity for logic analyzers	Perform time-domain, spectrum, and modulation quality analysis on digital Baseband and IF signals. www.keysight.com/find/dvsa
B4601C serial-to-parallel analysis package	Eliminate the tedious, time-consuming, and error-prone task of sifting through thousands of analysis package serial bits by looking at long vertical columns of captured 1's and 0's. The B4601C serial-to-parallel analysis package is general-purpose software that allows easy viewing and analysis of serial data.
B4602A signal extractor tool	This tool processes input signals and based on xml algorithms and creates a mapping of captured signals into new bus and signal names.
B4606A advanced customization environment–development and runtime package	Tailor your logic analyzer interface with a wide range of control, analysis and display capabilities specific to your measurement application. Create integrated dialogs, graphical displays and analysis functions to quickly manipulate measurement data into a format that provides additional insight and answers. www.keysight.com/find/logic-customview
B4607A advanced customization environment–runtime package	Run the macros and graphical views created with a B4606A development package or obtain and run a variety of commonly requested tools from Keysight and its partners to help customize your measurement environment.
B4608A ASCII remote programming interface	Remotely control a 16850-Series logic analysis system by issuing ASCII commands. This interface is designed to be as similar as possible to the RPI on the 16700 Series logic analysis system, so that you can reuse existing programs. Requires either B4606A or B4607A to be enabled. You can also use the B4606A to customize and add RPI commands.
B4610A data import package	Use the logic analyzer GUI to view data obtained from tools other than a logic analyzer.
B4630A MATLAB connectivity and analysis package	Make an easy connection to MATLAB and transfer your logic analyzer measurement data for processing. Display the results on the logic analyzer in an XY scattergram chart.

Validate your DDR2 and DDR3 Memory Systems

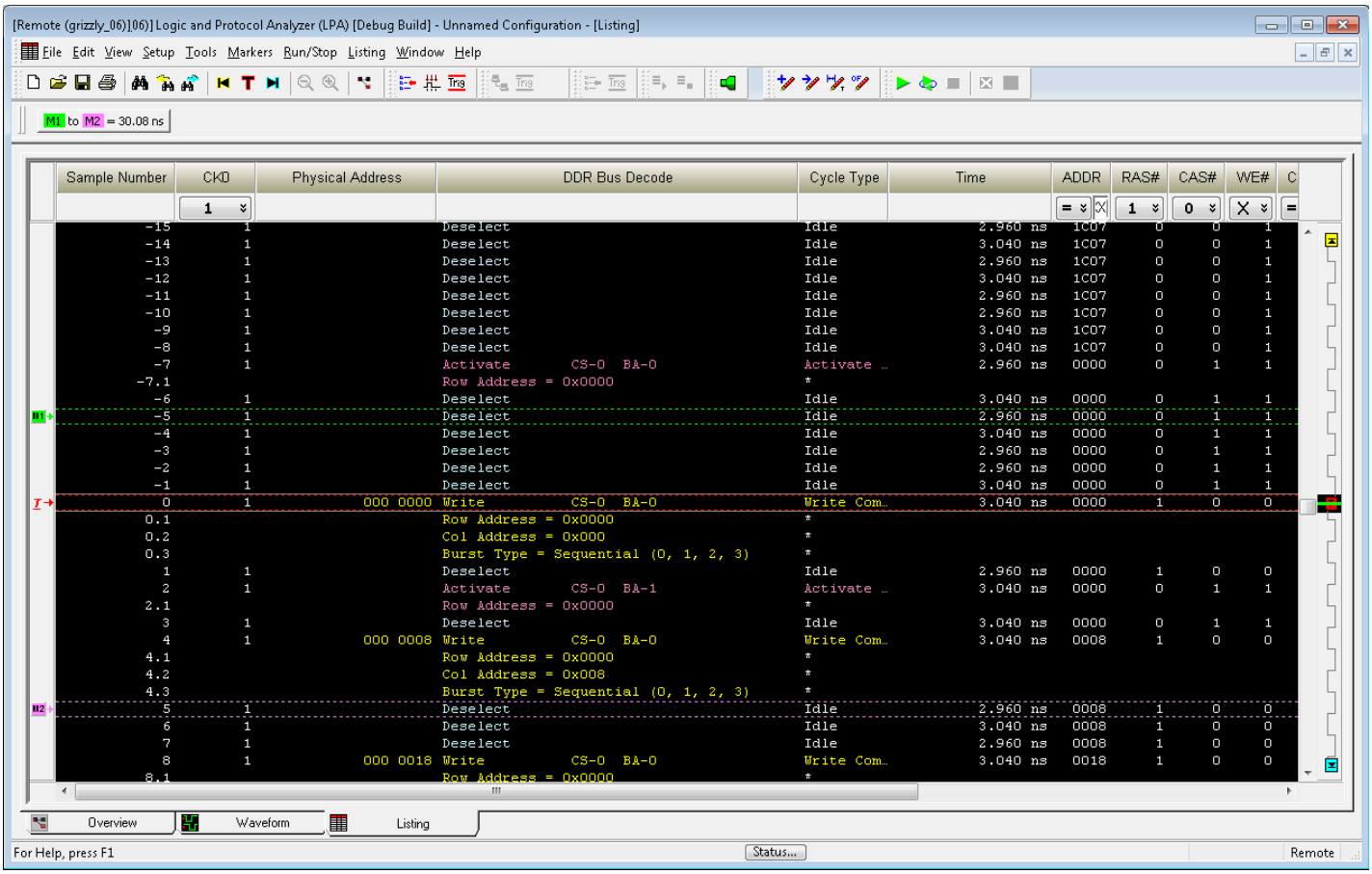
The state analysis capabilities of the 16850 Series allow it to make measurements and analysis on DDR2 and DDR3 memories up to DDR2/3 1333 (667 MHz clock) on address and control lines. Memory bus decode, compliance testing, and performance analysis are available in state mode only with related orderable tools.

	DDR2 memory	DDR3 memory
Addr/Cmd only	**Up to DDR2 1333 (667 MHz clock) state measurements on Addr/Cmd only. (No data)**	**Up to DDR3 1333 (667 MHz clock) state measurements on Addr/Cmd only. (No data)**
	Requires 34 channel model or higher (one U4201A cable required providing two 90 pin pods)	
	Related Orderable SW Tools (State mode only): – B4621B Bus Decoder for DDR, DDR2, DDR3, DDR4 Debug and Validation (Only DDR2 and DDR3 are supported with the 16850 Series logic analyzer.) – B4622B Protocol Compliance and Analysis Toolset for DDR/2/3/4, and LPDDR/2/3 (Only DDR2 and DDR3 are supported with the 16850 Series logic analyzer.)	
	Supported probes with configuration files: – x16 Addr/Cmd/Data DDR2 BGA probe (W2631B)(Requires E5384A ZIF probe) [1] – x8 Addr/Cmd/Data DDR2 BGA probe (W2633B)(Requires E5384A ZIF probe) [1]	Supported probes with configuration files: – x16 Addr/Cmd/Data DDR3 BGA probe (W3631A)(Requires E5845A ZIF probe) [1] – x8 Addr/Cmd/Data DDR3 BGA probe (W3633A) (Requires E5847A ZIF probe) [1]
		FS2372 DDR3 DIMM interposer (Addr/Cmd only)
		FS2374 DDR3 SODIMM interposer (Addr/Cmd only)
Addr/Cmd/Data	**Up to DDR2 800 (400 MHz clock) timing measurements** using 2.5 GHz timing analyzer with deep memory (for 3:1 ratio of sample rate to data rate)	**Up to DDR3 800 (400 MHz clock) timing measurements** using 2.5 GHz timing analyzer with deep memory (for 3:1 ratio of sample rate to data rate)
	Requires 68 channel model or higher (two U4201A cables using three of the four 90 pin pods provided)	
	Supported probes with configuration files: – x16 Addr/Cmd/Data DDR2 BGA probe (W2631B)(Requires E5384A ZIF probe) – x8 Addr/Cmd/Data DDR2 BGA probe (W2633B)(Requires E5384A ZIF probe)	Supported probes with configuration files: – x16 Addr/Cmd/Data DDR3 BGA probe (W3631A)(Requires E5845A ZIF probe) – x8 Addr/Cmd/Data DDR3 BGA probe (W3633A) (Requires E5847A ZIF probe)

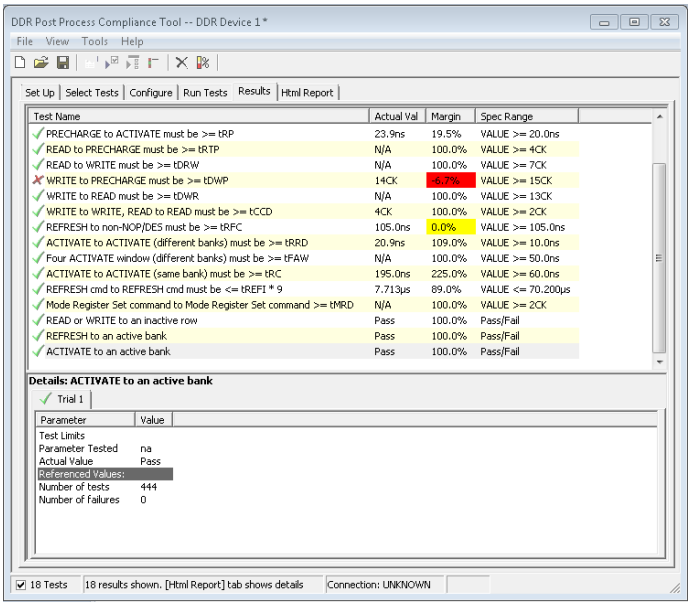
For higher speed memory analysis or greater channel count refer to the U4154A logic analyzer module.

1. Data pod is not connected for State measurements when used with the 16850 Series. Simultaneous State mode capture of Read and Write data requires a U4154A high-performance logic analyzer module with dual sample mode.

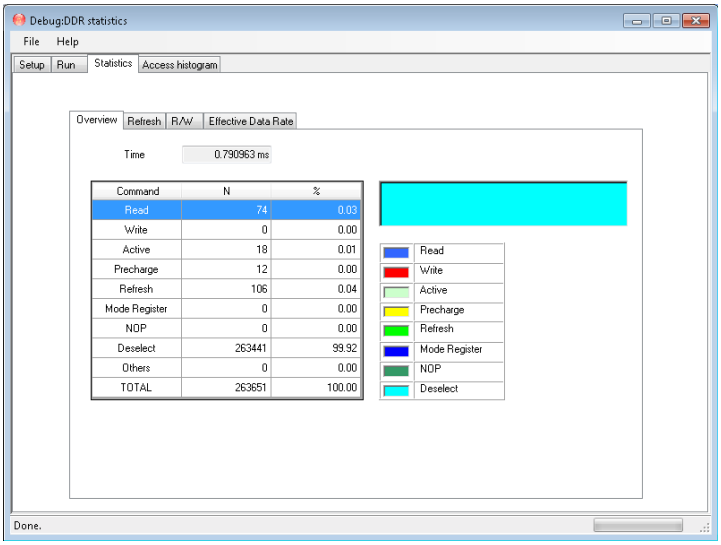
Validate your DDR2 and DDR3 Memory Systems (Continued)



16850 Series capture and decode of DDR3 Addr/Cmd lines



Compliance test analysis of DDR3 Addr/Cmd line saved trace



Performance test analysis of DDR3 Addr/Cmd line saved trace

Figure 5. Multiple views for DDR2 and DDR3 Addr/Cmd capture.

Deep Memory Capture with 2.5 GHz (400 ps Eesolution) Timing

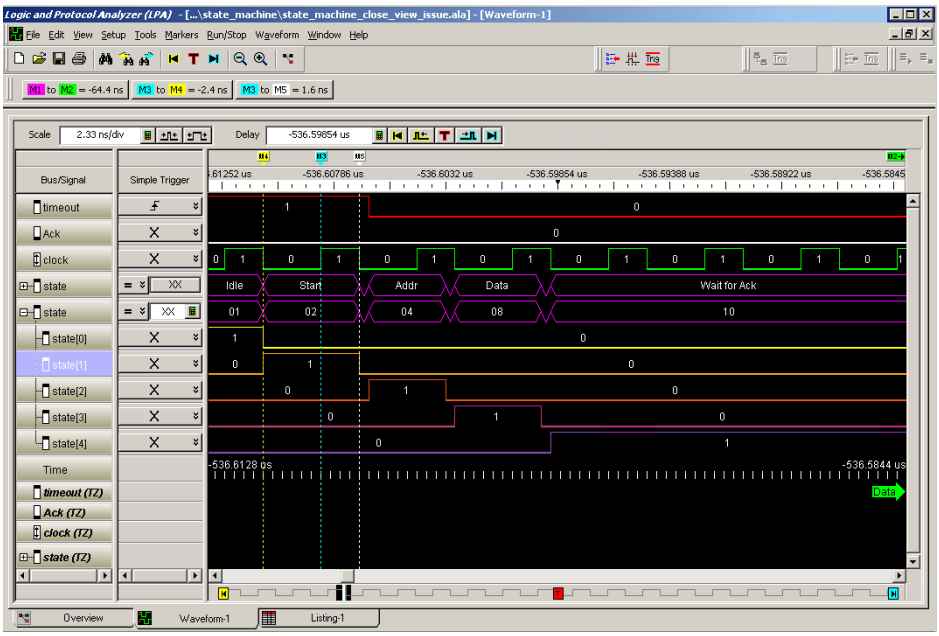


Figure 6. Timing mode capture with 400 ps resolution and up to 128 M samples memory depth (example capture at –500 µs before trigger).

Powerful, Customizable Triggering with a 1.4 GHz Sequencer

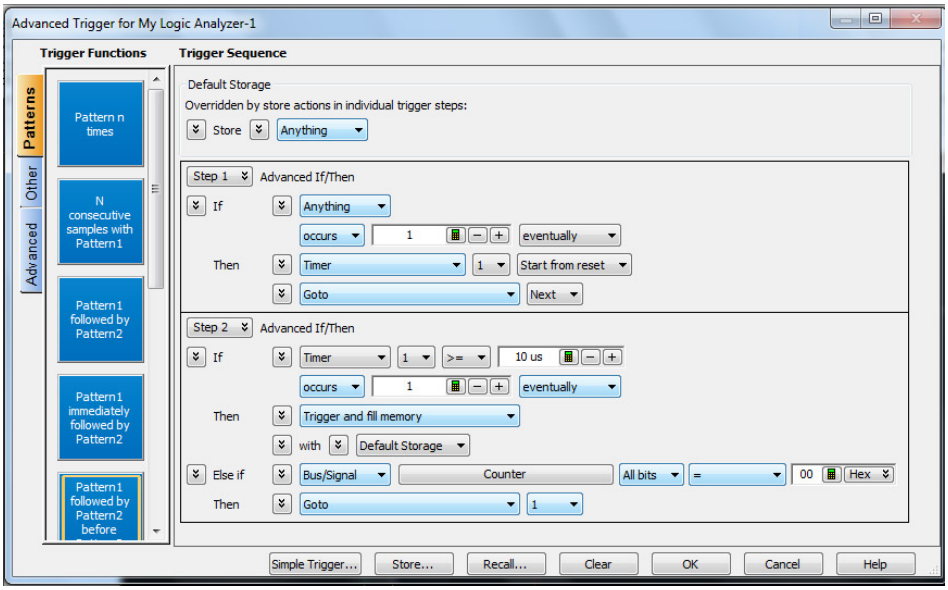


Figure 7. Example of a time out trigger to capture an error condition.

16850 Series Instrument Characteristics

Standard data views	
Waveform	Integrated display of data as digital waveforms, analog waveforms imported from an external oscilloscope, and/or as a chart of a bus' values over time
Listing	Displays data as a state listing
Compare	Compares data from different acquisitions and highlights differences
Source code	Displays time-correlated source code and inverse assembly simultaneously in a split display
	Define the trigger event by simply clicking on a line of source code
	Obtain source-code-level views of dynamically loaded software or code moved from ROM to RAM during a boot-up sequence using address offsets
	Requires access to source files via the LAN or instrument hard drive to provide source code correlation
	Source correlation does not require any modification or recompilation of your source code
Eye scan	Displays eye diagrams across all buses and signals simultaneously, allowing you to identify problem signals quickly
Data display	
Numeric bases for data display	Binary, hex, octal, decimal, signed decimal (two's complement), ASCII, symbols, and processor mnemonics
Symbolic support/object file format compatibility	
Number of symbols/ranges	Unlimited (limited only by amount of virtual memory available on 16850 Series logic analyzers)
Object file formats supported	IEEE-695, Aout, Omf86, Omf96, Omf386, Sysrof, ELF/DWARF1 $_1$, ELF/DWARF2 $_1$, ELF/Stabs1, ELF/Stabs2, ELF/Mdebug Stabs, TICOFF/COFF, TICOFF/Stabs
ASCII	GPA (general purpose ASCII)
User defined symbols	Specify a mnemonic for a given bit pattern for a label or bus
Available data/file formats	
ala	Contains information to reconstruct the display appearance, instrument settings, and trace data (optional) that were present when the file was created
xml	Extensible markup language for configuration portability and programmability
csv	CSV (comma-separated values) format for transferring data to other applications like Microsoft Excel
mfb	Export logic analyzer data for post-processing. Mfb data can be parsed using programming tools
Standard analysis tools	
Filter/colorize	Show, hide, or color certain samples in a trace for easier identification and analysis
Find (next/previous)	Locate specific data in a captured trace

16850 Series Instrument Characteristics (Continued)

16850 Series PC characteristics		
Operating system	Microsoft Windows 7 Embedded (64-bit)	
Processor	Core 2 Duo, M890, 3.0 GHz microprocessor	
Chipset	Intel Q45	
System memory	4 GB	
Removable hard disk drive	500 GB	
Installed on hard drive	Operating system, latest revision of the logic and protocol application software, optional application software ordered with the logic analyzer	
16850 Series instrument controls		
LCD touch-screen display	Large 38.1-cm (15-in.) touch-screen display makes is easy to view a large number of waveforms or states	
Front-panel hot keys	Dedicated hot keys for selecting run mode and disabling touch screen	
Front-panel knob	General-purpose knob adjusts viewing and measurement parameters	
Keyboard and mouse	PS/2 keyboard and USB mouse	
16850 Series video display modes		
Touch-screen display standard	Size	38.1 cm (15 in.) diagonal
	Resolution	1024 x 768
External display	Simultaneous display capability	Front panel and external display can be used simultaneously at 1024 x 768 resolution
	Supports up to four external monitors at up to 1600 x 1200 (with PCI video card)	

Programmability

You can write programs to control the logic analyzer application from remote computers on the local area network using COM or ASCII.

The COM automation server is part of the logic analyzer application. This software allows you to write programs to control the logic analyzer. All measurement functionality is controllable via the COM interface.

The B4608A Remote Programming Interface (RPI) lets you remotely control a 16850 Series logic analyzer by issuing ASCII commands to the TCP socket on port 6500. This interface is designed to be as similar as possible to the RPI on 16700 Series logic analysis systems, so that you can reuse existing programs.

The remote programming interface works through the COM automation objects, methods, and properties provided for controlling the logic analyzer application. RPI commands are implemented as Visual Basic modules that execute COM automation commands, translate their results, and return proper values for the RPI. You can use the B4606A advanced customization environment to customize and add RPI commands.

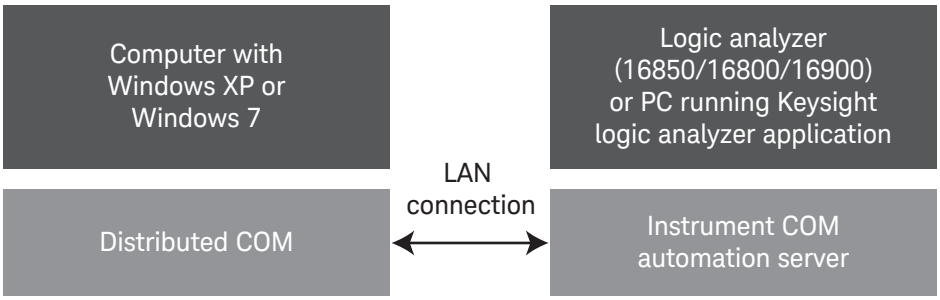


Figure 8. 16850 Series programming overview.

16850 Series Interfaces

Peripheral interfaces	
Display	One 15-pin XGA connector and one DVI connector
Keyboard	PS/2
Mouse	PS/2
Serial	9-pin D-sub
PCI card expansion slot	1 full profile
Audio ports	Line in, line out, mic in
USB	Six 2.0 ports, two in front, four in rear
Connectivity interfaces	
LAN	10Base-T, 100Base-T, 1000Base-T
Connector	RJ-45
Interface with external instrumentation	
Trigger or arm external devices or receive signals that can be used to arm measurement hardware within the logic analyzer with Trigger In/Out	
Trigger in	
Input	Rising edge or falling edge
Action taken	When received, the logic analyzer takes the actions described in the trigger sequence step
Input signal level	± 5 V max
Threshold level	Selectable: ECL, LVPECL, LVTTL, PECL, TTL
	User defined (± 5 V in 50 mV increments)
Minimum signal amplitude	200 mV
Connector	BNC
Input resistance	4 kΩ nominal
Trigger out	
Trigger	Rising edge or falling edge. OR of selected events that cause Trigger Out (logic analyzer trigger or flags)
Output signal	VOH (output high level) 2.0 V min
	VOL (output low level) 0.5 V max
	Pulse width approx. 80 to 160 ns
Threshold level	LVTTL (3.3 V logic)
Signal load	50 Ω (For good signal quality, the trigger out signal should be terminated in 50 Ω to ground)
Connector	BNC

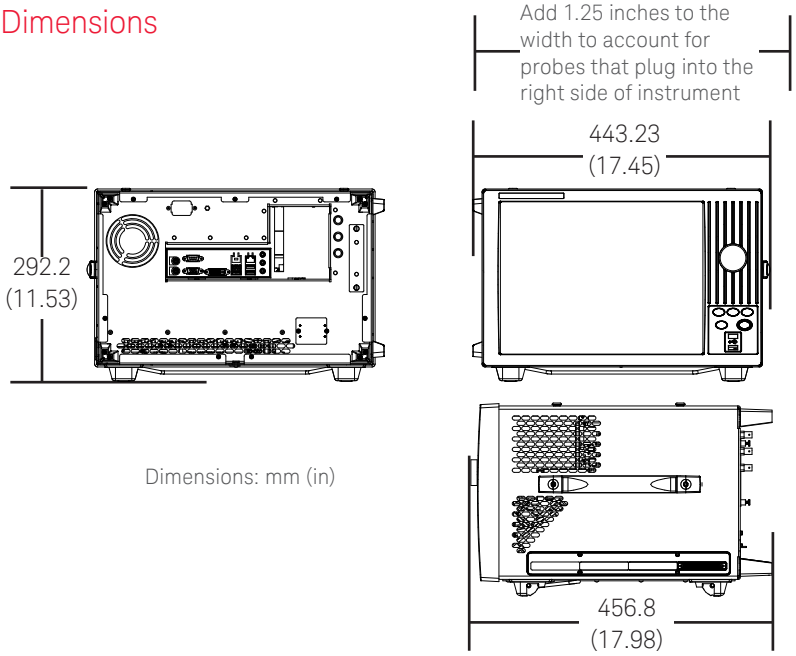
16850 Series Physical Characteristics

Power	
16851A	100 to 240V ± 10 %, 50/60Hz, 400 W max
16852A	100 to 240V ± 10 %, 50/60Hz, 400 W max
16853A	100 to 240V ± 10 %, 50/60Hz, 400 W max
16854A	100 to 240V ± 10 %, 50/60Hz, 400 W max

Note:

- The mains supply voltage fluctuations are not to exceed ± 10 % of the nominal supply voltage.
- Add 1.25 inches to the width to account for probes that plug into the right side of instrument.

Dimensions



Dimensions: mm (in)

Figure 9. 16850 Series exterior dimensions.

Weight	Max net	Max shipping
16851A	15.0 kg (33.0 lbs)	21.7 kg (48 lbs)
16852A	15.0 kg (33.0 lbs)	21.7 kg (48 lbs)
16853A	15.0 kg (33.0 lbs)	21.7 kg (48 lbs)
16854A	15.0 kg (33.0 lbs)	21.7 kg (48 lbs)

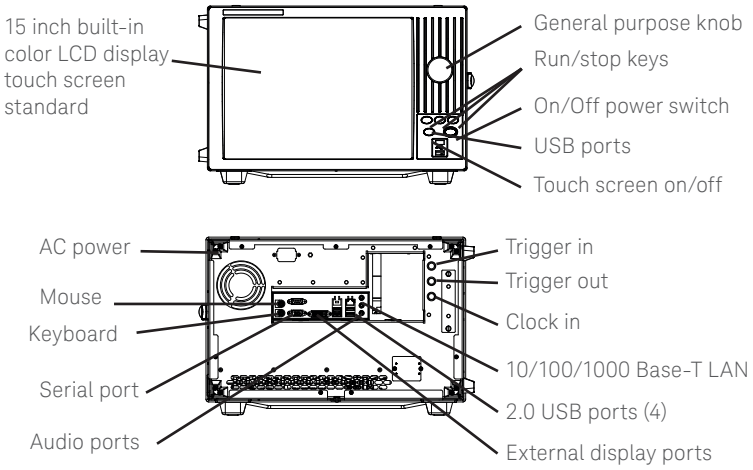


Figure 10. 16850 Series front and back panels.

Instrument operating environment	
Temperature	5 °C to 40 °C (41 °F to 104 °F)
Altitude	To 2000 m (6,561 ft)
Humidity	Maximum 80% relative humidity, non-condensing

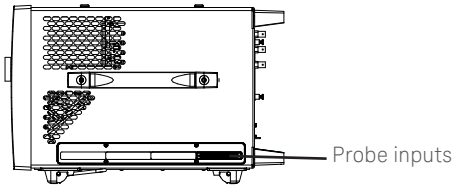


Figure 11. 16850 Series side view.

Extra notes regarding the 16850 Series:

1. Pollution degree 2;
2. Installation category II;
3. These instruments are intended for use in an indoor lab environment

Ordering Information

Each 16850 Series portable logic analyzer comes with one USB keyboard, one USB mouse, accessory pouch and power cord. Selecting a logic analyzer to meet your application and budget is as easy as 1, 2, 3.

1 Choose the channel count				
Model	**16851A**	**16852A**	**16853A**	**16854A**
Channels	34	68	102	136

2 Choose the state speed	
State speeds	350 MHz state clock; 700 Mbps data rate: Standard
	700 MHz state clock; 1.4 Gbps data rate: < Model number > -700

3 Choose the memory depth	
Memory depth (samples)	2 Mb: Standard
	4 Mb: < Model number > -004
	8 Mb: < Model number > -008
	16 Mb: < Model number > -016
	32 Mb: < Model number > -032
	64 Mb: < Model number > -064
	128 Mb: < Model number > -128

16850 Series Probing Options

Logic analyzer probes are ordered separately. Please specify probes when ordering to ensure the correct connection between your logic analyzer and the device under test.

16850 Series logic analyzer probes	
General-purpose flying lead probes	
U4203A	34-ch single-ended data, differential clock, direct connect
E5381B	17-ch differential probe for 90 pin LA pod [1, 2]
E5382B	17-ch single-ended probe for 90 pin LA pod [1, 2]
Connectorless probes	
U4204A	**Soft Touch Pro Series:** 34-ch single-ended data, differential clock, direct connect
E5387A	**Soft Touch Classic Series:** 17-ch differential for 90 pin LA pod [1, 2]
E5398A	**Half-Size Soft Touch:** 17-ch single-ended for 90 pin LA pod [1, 2]
E5390A	**Soft Touch Classic Series:** 34-ch single-ended for 90 pin LA pod [1, 3]
E5405B	**Soft Touch Pro Series:** 17-ch differential for 90 pin LA pod [1, 2]
E5406A	**Soft Touch Pro Series:** 34-ch single-ended for 90 pin LA pod [1, 3]
Connector probes	
U4201A	34-ch logic analyzer cable for use with E5xxxA 90-pin probes
U4205A	**Mictor:** 34-ch single-ended data and clock, direct connect
E5378A	**Samtec:** 34-ch single-ended probe for 90 pin LA pod [1, 3]
E5379A	**Samtec:** 17-ch differential probe for 90 pin LA pod [1, 2]
E5380B	**Mictor:** 34-ch single-ended probe for 90 pin LA pod [1, 2]

1. Logic analyzer probe used with the U4201A logic analyzer cables.
2. 17 channel probes require one of two 90 pin pods provided on the U4201A logic analyzer direct connect cable.
3. 34 channel probes require both 90 pin pods provided on the U4201A logic analyzer cable.

Additional 16850 Series Options

Keysight product or option number	Description	Ordering information
E5864A	Additional external hard drive (imaged with operating system and logic analyzer application software)	E5864A

After Purchase Options

Upgrade memory depth or state speed after purchase				
Logic analyzer channels	34	68	102	136
Logic analyzer models	16851A	16852A	16853A	16854A
After purchase upgrade model numbers	16851AU	16852AU	16853AU	16854AU
Memory depth (samples)	4 M: < Upgrade model number > -004			
	8 M: < Upgrade model number > -008			
	16 M: < Upgrade model number > -016			
	32 M: < Upgrade model number > -032			
	64 M: < Upgrade model number > -064			
	128 M: < Upgrade model number > -128			
State speed	700 MHz state clock/1400 Mbps state data rate: < Upgrade model number > –700			

Related Literature

Publication title	Publication number
16850 Series Portable Logic Analyzers - Product Fact Sheet	5991-2836EN
16900 Series Logic Analysis Systems - Brochure	5989-0420EN
Measurement Modules for the 16900 Series - Data sheet	5989-0422EN
B4655A FPGA Dynamic Probe for Xilinx - Data Sheet	5989-0423EN
Probing Solutions for Logic Analyzers - Data Sheet	5968-4632E

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